# SR ENGINEERING COLLEGE

(Autonomous institution)



# Hand Book IV-B.Tech I-Sem Electronics and Communication Engineering

RA-13 Regulation Course Accredited by NBA, Accredited by NAAC with 'A' Grade, Approved by AICTE, Affiliated to JNTU, Hyderabad

Ananthasagar, Warangal, Telangana – 506 371

I Semester: 12-06-2017 to 13-10-2017

#### **SR Educational Group**

The thirst for knowledge and the enthusiasm to go beyond and think 'out of the box' is something that S R group encourages, nurtures and supports among our students.

**S R Engineering College**, Warangal was established in 2002 by S R Educational Society. It is located on Warangal-Karimnagar highway at about 15 KM away from Warangal City. The college is affiliated to JNTU, Hyderabad. It is running 5 undergraduate (B.Tech) and 7 postgraduate (M.Tech) engineering programs besides, Master of Business Administration (MBA). Three undergraduate engineering programs are accredited by the National Board of Accreditation (NBA) within a short span of six years of its establishment. The college was recently sanctioned with two new integrated programs; a 5-year dual degree program in Management (BBA+MAM) and a 5½ year dual degree program in engineering (B.Tech+MTM). The college is granted Autonomous Status by University Grants Commission (UGC) in 2014.

S R Engineering College (SREC) is an autonomous and accredited institution valuing and encouraging creativity and quality in teaching and research. The staff and the students take on new and interesting activities to acquire ability to think uniquely and independently. The college is in a position to attract and develop outstanding faculty to actively participate and interactively support an open academic climate in the campus. It adopts innovative approaches for continuous improvement by strategic planning, benchmarking and performance monitoring. The policy is to establish a system of quality assurance of its graduates by continuously assessing and upgrading teaching and learning practices.

Through active industry cooperation, SREC has established centers like CISCO Networking Academy, Microsoft Innovation Centre, IBM Centre of Excellence and NEN Centre for Entrepreneurship Development for nurturing specific skill sets for employability. To shape and transform the graduates to meet challenging and complex engineering tasks globally, the college has built and fostered relationship with reputed universities like University of Massachusetts, Saint Louis University, University of Missouri and Wright State University. To align with ABET system of outcome based curriculum, many reforms have been implemented in the course structure with due stress on basic sciences and humanities, interdisciplinary and core engineering including projects and seminars in line with AICTE guidelines.

The college is striving to create and support academic and research activities in thrust areas like energy and environment. The institute has reliable, flexible and scalable technology infrastructure for networking and web services which provides crucial support for improved functioning and timely service to students and faculty. The centre for student services and placements (CSSP) actively pursues training and campus placements by keeping in touch with industry for internships and employment. The faculty is highly motivated to advance their knowledge and qualifications through sponsored research. The digital library provides the necessary resources and e-learning services. Regular seminars, webinars, workshops and conferences and faculty development programs are conducted to encourage participation from students and faculty from neighboring colleges.

S R Engineering College is implementing a strategic action plan with specific focus on:

- 1. Novel technology enabled teaching and learning techniques,
- 2. Strengthen existing PG programs through modernization of laboratories and training of faculty and staff,
- 3. Identify and start new PG programs in current areas of research with immediate relevance to the state and the country,
- 4. Attract funding for sponsored research from DST, MNRE, AICTE and UGC,
- 5. Strengthen functional areas like governance and administration, infrastructure, finance etc.,
- 6. Network with industry and institutes of repute through academic partnership for expanding avenues for internships and research.

# VISION

To be among the Top 20 Private Engineering Institutes in India by 2020

# **MISSION**

- Design and implement curriculum that equips students with professional and life skills
- Recruit, develop and retain outstanding faculty to achieve academic excellence
- Promote and undertake quality research in thrust areas of science and Technology
- Collaborate with industry and academia to meet the changing needs of society
- Foster innovation and cultivate the spirit of entrepreneurship among students

# **About The Department**

The Department of ECE is one of the biggest department in the college with highly experienced, qualified, dedicated, and trained faculty with deep sense of commitment towards the Students and Institution. The department has 56 staff members, 5 of whom are Doctorates and 12 faculties are pursuing their higher qualifications from various universities besides this most of the faculty were executing research projects from various funding agencies like AICTE, DST and UGC The main research of the department is in the area of VLSI, Embedded Systems and Communications. The department has four major projects from Department of Science and Technology and one minor project from UGC. The department of ECE has well equipped and state of the art laboratories for both UG & PG programs. To cater the needs of the students several technical talks, workshops, personality development programs, soft skills and entrepreneurial activities are regularly conducted under professional societies besides the curriculum. The Department has an Active IEEE student branch and IETE Student forum.

The department has its own Vision and Mission at par with the Vision and Mission of the Institute.

# VISION

To be the leading Electronics and Communication Engineering Department in promoting quality education, research and consultancy

# MISSION

- Design curriculum that provides effective engineering education by promoting innovating teaching-learning practices
- Establish centers of excellence in core areas and take up consultancy and research
- Interact and work closely with industries, research organizations to accomplish technology transfer
- Impart necessary skills and promote professional practices to enhance placement and entrepreneurship

# **Program Educational Objectives (PEOs)**

PEOs (Program Educational Objectives) relate to the career and professional accomplishments of students after they graduate from the program. Consequently, assessment and evaluation of the objectives requires assessment tools that can be applied after graduation.

- Enhance the skill set of students by providing strong foundation in basic sciences, mathematics, engineering and use necessary tools to solve engineering problems..
- II. Equip students with ethical, professional behavior and mould them to become successful qualified engineers.
- III. Inculcate necessary aptitude and ability to equip students to use their knowledge as a foundation for lifelong learning.
- IV. Build team work skills and develop abilities to communicate and deal with different professionals both nationally and globally.

#### **Program Outcomes (POs):**

Engineering Graduates will be able to:

- 1. **Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- 2. **Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- 3. **Design/Development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- 4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- 5. **Modern Tools usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
- 6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- 7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- 8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- 9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- 10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- 11. **Project Management and Finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- 12. Life Long Learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

# Academic Calendar for II - IV B. Tech. I & II Semester Academic Year 2017 – 18

## <u>I Semester</u>

S. No.	Description	Schedule	Duration
1	Commencement of Class work	12.06.2017	
2	1 <sup>st</sup> Spell of Instruction	12.06.2017 to 05.08.2017	8 Weeks
3	1 <sup>st</sup> Mid Examinations <i>Timings:</i> FN: 10.00 am to 11.30 am : AN:2.00 pm to 3.30 pm	08.08.2017 to 10.08.2017	3 Days
4	2 <sup>nd</sup> Spell of Instruction (Includes Dasara Holidays)	11.08.2017 to 11.10.2017	9 Weeks
6	2 <sup>nd</sup> Mid Examinations <i>Timings:</i> FN: 10.00 am to 11.30 am : AN:2.00 pm to 3.30 pm	12.10.2017 to 16.10.2017	3 Days
7	End Semester Regular Examinations / Supplementary Examinations (Theory & Practical)	17.10.2017 to 02.12.2017	7 Weeks
8	Commencement of Class work for II, III, IV B.Tech. II Sem. for the academic year 2016- 2017	04.12.2017	

# **COUSE STRUCTURE**

#### **IV Year I Semester**

Sl.	Course	Course	L	Т	P/D	С	Ma	arks
No.	Code	course	Ľ	•	1/D	C	Int.	Ext.
1	13EC427	Microwave Engineering	4	1	-	4	30	70
2	13EC428	VLSI Design	4	1	-	4	30	70
3	13EC429	Electronic Measurements and Instrumentation	3	1	-	3	30	70
4	13EC430	Computer Networks	3	1	-	3	30	70
5	13EC431A 13EC431B 13EC431C	<b>Professional Elective – I</b> Digital System Design Embedded Systems Satellite Communications	3	1	-	3	30	70
6	13EC432A 13EC432B 13EC432C	<b>Professional Elective – II</b> Digital Image Processing DSP Processors and Architecture Bio-Medical Instrumentation	3	1	-	3	30	70
7	13EC436	Microwave Engineering and Digital Communications Laboratory	-	-	3	2	25	50
8	13EC437	E-CAD and VLSI Laboratory	-	-	3	2	25	50
9	13EC438	Industry Oriented Mini-project	-	-	-	1	30	20
	Total					25	8	00

# TIME TABLE

# **Dept. of Electronics and Communication Engg.**

SR ENGINEERING COLLEGE, Ananthasagar, Warangal CLASS TIME TABLE Academic year 2017-18 (I-SEM)

Class:I	V-ECE-A			Room N	o: 2301			w.e.f.12	-06-2017	
Day	9:30- 10:20	10:20- 11:10	11:10- 11:20	11:20-12:10	12:10-1:00	1:00-1:40	1:40-2:30	2:30-3:15	3:15-4:00	
Day	Ι	Π	DDEAK	III	IV		v	VI	VII	
MON	MWE	ES	BREAK	CN	VLSI		EMI	DSPA	CN	
TUE	VLSI		MWE/	MWE/VLSI Lab			ES	CN	MWE	
WED	ES	DSPA		MWE	EMI	LUNCH BREAK	VLSI	CED		
THU	EMI	MWE	BRI	VLSI	DSPA	<b>EAK</b>	М	WE/VLSI I	Lab	
FRI	CN	DSPA	BRE     VLSI     DSPA       VLSI     EMI		MWE	ES	Sports/ Library			
SAT	DSPA	VLSI		EMI	ES					

Class Teacher: Mr. J. Ravichander

#### Subjects:

MWE: Microwave Engineering (13EC424) :Ms. Ishita

VLSI: VLSI Design (13EC425): Dr. Ajay Kumar

EMI: Electronic Measurements and Instrumentation (13EC426): Mr. B. Girirajan

ES: Embedded System (13EC429): Ms. P. Anuradha

DSPA: DSP Processors and Architecture (13EC432): Ms. G. Renuka

CN: Computer Networks(13EC427) : Mr. J. Ravichander

## Labs:

MEW & DC Lab: Microwave Engineering & Digital Communication Lab (13EC443):

Ms. Ishista / Mr. K. Naveen

ECAD & VLSI Lab (13EC444): Dr. Ajay Kumar / Ms. Navya Jyothi

#### Dept. of Electronics and Communication Engg. SR ENGINEERING COLLEGE, Ananthasagar, Warangal CLASS TIME TABLE Academic year 2017-18 (I-SEM)

Class	:IV-ECE-B	8	1	Room N	No: 2302			w.e.f.12	-06-2017
D	9:30-10:20	10:20-11:10	11:10-11:20	11:20-12:10	12:10-1:00	1:00-1:40	1:40-2:30	2:30-3:15	3:15-4:00
Day	Ι	II		III	IV		V	VI	VII
MON	EMI	VLSI		DSPA	MWE		MV	VE/VLSI L	ab
TUE	ES	CN	BREAK	MWE	EMI	EMI EN		ES DSPA	
WED	MWE	EMI		VLSI	ES	CH BI	CN	CED	ED
THU	VLSI	ES		MWE	CN	LUNCH BREAK	DSPA	EMI	Sports/L ibrary
FRI	DSPA		MWE/V	LSI Lab			CN	VLSI	MWE
SAT	CN	EMI	BREAK	VLSI	DSPA				

Class Teacher: Mr. K. Sreedhar

## Subjects:

MWE: Microwave Engineering (13EC424): Mr. K. Sreedhar

VLSI: VLSI Design (13EC425): Dr. K. Swaminathan

EMI: Electronic Measurements and Instrumentation (13EC426): Mr. B. Girirajan

ES: Embedded System (13EC429): Mr. A. Rajeshwar Rao

DSPA: DSP Processors and Architecture (13EC432): Mr. P. Krishna

CN: Computer Networks(13EC427) : Mr. J. Ravichander

#### Labs:

MEW & DC Lab: Microwave Engineering & Digital Communication Lab (13EC443):

Mr. K. Sreedhar / Mr. K. Naveen

ECAD & VLSI Lab (13EC444): Dr. K. Swaminathan / Ms. Navya Jyothi

# **Dept. of Electronics and Communication Engg.**

#### SR ENGINEERING COLLEGE, Ananthasagar, Warangal CLASS TIME TABLE Academic year 2017-18 (I-SEM)

	Class	: IV-ECE	- C	Roo	m No: 2206	<u> </u>	w.e.f. 1	2-06-2017	
Dari	9:30-10:20	10:20-11:10	11:10-11:20	11:20-12:10	12:10-1:00	1:00-1:40	1:40-2:30	2:30-3:15	3:15-4:00
Day	Ι	II		III	IV		V	VI	VII
MON	EMI	VLSI	BRF	CN	ES		MWE	CN	DSPA
TUE	ES	DSPA	BREAK	MWE	VLSI	LUNG	Μ	WE/VLSI I	.ab
WED	VLSI	ES		MWE	DSPA	LUNCH BREAK	EMI	CH	ED
THU	EMI		MWE/V	LSI Lab		REAK	MWE	VLSI	CN
FRI	MWE	CN	BREAK	DSPA	EMI		ES	VLSI	Sports/ Library
SAT	DSPA	EMI	EAK	CN	VLSI				

Class Teacher: Dr. A. Subbarao

#### Subjects:

MWE: Microwave Engineering (13EC424): Dr. A. Subbarao

VLSI: VLSI Design (13EC425): Dr. Bhanu Pratap Singh D

EMI: Electronic Measurements and Instrumentation (13EC426): Mr. Leo Joseph

ES: Embedded System (13EC429): Mr. P. Goverdhan

DSPA: DSP Processors and Architecture (13EC432): Ms. B. Saritha

CN: Computer Networks(13EC427) : Mr. P. Krishna

#### Labs:

MEW & DC Lab: Microwave Engineering & Digital Communication Lab (13EC443):

Dr.A.Subbarao / Ms. K. Priyanka

ECAD & VLSI Lab (13EC444): Dr. Bhanu Pratap Singh / Ms.N.Shilpa /Ms. P. Anjali

#### (13EC432B) DSP PROCESSORS AND ARCHITECTURE

#### **Course Description:**

DSPs are processors or microcomputers whose hardware, software and instruction sets are optimized for high-speed numeric processing applications an essential for processing digital data representing analog signals in real time. The DSP's high-speed arithmetic and logical hardware is programmed to rapidly execute algorithms modeling the filter transformation. The combination of design elements arithmetic operators, memory handling, instruction set, parallelism, data addressing that provide this ability forms the key difference between DSPs and other kinds of processors. Understanding the relationship between real-time signals and DSP calculation speed provides some background on just how special this combination is. The real-time signal comes to the DSP as a train of individual samples from an analog-todigital converter (ADC). To do filtering in real-time, the DSP must complete all the calculations and operations required for processing each sample (usually updating a process involving many previous samples) before the next sample arrives. To perform high-order filtering of real-world signals having significant frequency content calls for really fast processors. To get an idea of the type of calculations a DSP does and get an idea of how an analog circuit compares with a DSP system, one could compare the two systems in terms of a filter function. The familiar analog filter uses resistors, capacitors, inductors, amplifiers. It can be cheap and easy to assemble, but difficult to calibrate, modify, and maintain a difficulty that increases exponentially with filter order. For many purposes, one can more easily design, modify, and depend on filters using a DSP because the filter function on the DSP is softwarebased, flexible, and repeatable.

#### Prerequisites

Requires the knowledge of Signals and systems, Digital Signal Processing and fundamentals of computer architecture.

#### **Course Objectives**

- 1. Recall Digital Signal Processing and classify various computational errors in DSP.
- 2. Interpret basic Architecture for programmable DSP devices.
- 3. Learn the Architecture and programming of TMS320C6x Processors.
- 4. Implement DSP algorithm for digital filters.
- 5. Analyze various DSP interfacing techniques.

#### **Course Outcomes**

- 1. Represent real world signals in digital format.
- 2. List various computational errors in DSP.
- 3. Differentiate various Programmable architectures.
- 4. Develop programming of TMS320C6x Processors.
- 5. Construct various Digital filters.
- 6. Compute signal spectrum.
- 7. Interpret various DSP interfacing techniques
- 8. Build interface using MCBSP.

#### UNIT – I

**Computational Accuracy in DSP Implementations:** Introduction, A Digital signal processing system, Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

#### UNIT – II

**Architectures for Programmable DSP Devices:** Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

#### UNIT – III

**Execution Control and Pipelining:** Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

#### $\mathbf{UNIT} - \mathbf{IV}$

**Programmable Digital Signal Processors:** Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

#### UNIT – V

**Implementations of Basic DSP Algorithms and Interfacing:** The Q-notation, FIR Filters, IIR Filters, An FFT algorithm for DFT Computation, Computation of the signal spectrum, Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct Memory Access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example

#### **TEXT BOOKS:**

- 1. Avtar Singh and S. Srinivasan, "Digital Signal Processing", Thomson Publications, 2004. ISBN 10:81-315-0034-9, ISBN 13:978-81-315-0034-7
- 2. Lapsley et al. "DSP Processor Fundamentals, Architectures & Features", S. Chand & Co, 2000. *ISBN* 0-9660176-3-3

#### **REFERENCE BOOKS:**

- 1. B. Venkata Ramani and M. Bhaskar, "Digital Signal Processors, Architecture, Programming and Applications", TMH, 2004. *ISBN*: 9780070702561
- 2. Jonatham Stein, "Digital Signal Processing", John Wiley, 2005. ISBN 0-471-29546-9

#### WEBSITES

- 1. www.ti.com
- 2. www.mathworks.in
- 3. www.interfacebus.com
- 4. bwrcs.eecs.berkeley.edu/Classes/CS252/Notes/Lec10a-DSP1.pdf
- 5. www.dspguide.com/ch28/3.htm
- 6. opencores.org
- 7. www.dspguide.com/ch28/3.htm
- 8. www.analog.com

#### **CONTENT BEYOND SYLLABUS:**

- 1. Introduction to 3-D signals Processing.
- 2. 16 point DFT computation.

# LECTURE PLAN

Sl. No.	Topics in syllabus	Modules and Sub modules	Lecture No.	Suggested books with Page Nos.
UNIT	Γ – I Introduction to D	igital Signal Processing (No. of Lectu	ures – 10)	
1	An overview of DSP	Introduction, explanation of DSP system block diagram.	L1 L2	Avtar singh 1,2,7
2	Number formats for signals & coefficients in DSP systems	Fixed point ,Double precision point, floating point, block floating point format.	L3 L4	43-47
3	Dynamic Range and Precision	Dynamic Range, resolution and Precision Related problems.	L5 L6	47-49
4	Sources of errors	Sources of error in DSP implementations,	L7 L8	49
5	A/D Conversion errors	A/D Conversion errors, DSP Computational errors,	L9	49-54
6	D/A Conversion Errors	D/A Conversion Errors, Compensating filter.	L10	54-58
UNIT	<b>-II</b> Architectures for	Programmable DSP Devices (No. of ]	Lectures –	14)
7	Basic Architectural features	Basic Architectural features, DSP Computational Building Blocks.	L11 L12	61-63
8	DSP Computational Building Blocks	Parallel multiplier, shifter, MAC unit,ALU	L13 L14 L15	63-76
9	Bus Architecture and Memory,	Von Neumann, Harvard architecture, on chip memory	L16	77-80
10	Data Addressing Capabilities	Immediate,register,direct,indirect, special Addressing modes	L17 L18	81-90
11	Address Generation Unit	Address Generation Unit	L19	90-91
12	Programmability and Program Execution	Program control and sequencer	L20 L21	91-95
13	Speed Issues	Parallelism, Pipelining	L22 L23	95-101
14	Features for External	Features for External interfacing.	L24	102
UNIT	Γ-III Execution Cont	ol and Pipelining (No. of Lectures –	· <b>07</b> )	
				nentals by phil lapsley
15	Hardware looping		L25	91-94

16	Interrupts, Stacks.		L26	94-98
17	Relative Branch supp	port.	L27	98
18	Pipelining and Interlocking.	Performance, Pipeline Depth,	L28 L29	99-104
19	Branching effects, In	terrupt effects.	L30	104-108
20	Programming models	5.	L31	108
UNIT	Γ – IV Programmable I	Digital Signal Processors: (No. of Lec	tures – 12	)
21	Commercial Digital signal-processing Devices	Introduction to TMS320C54XX DSPs, Bus structure.	L32 L33	Avtar singh 107-117
22	Data Addressing modes	Immediate,absolute,accumulator, direct,indirect,memory mapped, stack	L34 L35 L36	117-129
23	Memory space	Memory map of 5416	L37	129-131
24	Program Control, instructions and Programming	Instruction Set of 54xx	L38 L39	132-137
25	On-Chip Peripherals	Hardwaretimer,HPI,clock generator, serial I/O ports	L40 L41	142-146
26	Interrupts	Interrupt locations and priorities	L42	146-147
27	Pipeline Operation	Pipeline Operation of 54xx	L43	148-150
UNI	Γ–V Implementations	of Basic DSP Algorithms and Interfac	ing (No. of	Lectures – 16)
28	The Q-notation, FIR Filters, IIR Filters	Problems on Q-notation filter implementations.	L44 L45	176-187
29	An FFT algorithm for DFT Computation	8 point DFT computation	L46	215-219,224-232
30	Computation of the signal spectrum,	Overflow ,scaling	L47 L48	219-223,233
31	Memory space organization.	Memory map of 5416	L49	236-238
32	External bus interfacing signals	Memory and I/O interfacing signals	L50	238-240
33	Memory interface, Parallel I/O interface.	Wait states, design examples	L51 L52	240-245

34	Programmed I/O, Interrupts and I/O.	Timing diagrams, flow chart	L53 L54	245-255
35	Direct Memory Access (DMA).	DMA operation, register sub addressing	L55	255-259
36	A Multichannel buffered serial port (McBSP).	Block diagram of c54xx	L56 L57	264-266
37	a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example	Details of PCM3002CODEC	L58 L59	266-272

#### **Review Questions**

#### UNIT – I

- 1. Explain with a block diagram a basic DSP system? What are the advantages and disadvantages of programmable DSP processors?
- 2. Mention various Number formats for signals and coefficients in DSP systems
- 3. Define Dynamic Range and Precision.
- 4. Explain the Sources of error in DSP implementations.
- 5. Explain A/D Conversion errors and DSP Computational errors.
- 6. Write about D/A Conversion Errors and Compensating filter.

## UNIT – II

- 1. Draw the architecture for buses and memory in DSP processors and explain.
- 2. Explain in detail the features of external interfacing of DSP processor.
- 3. What are the DSP computational building blocks and Explain about MAC.
- 4. Explain the structure of:
  (a) 4 × 4 Broun multiplier and
  (b) Barrel shifter for 4-bits.
- 5. Differentiate Von Neumann architecture and Harvard architecture.
- 6. Draw the block diagram of address generation unit and explain it.
- 7. Explain briefly about speed issues.
- 8. Write about programmability and program execution of DSP devices.
- 9. Compute the sequence in which the input data should be ordered for a 16- point DIT-FFT.
- 10. DSP has a circular buffer with start & end addresses as 0200h,020fh respectively. What would be the new values of the address pointer of the buffer, it gets updated to 0212h, 01fch.

#### UNIT – III

- 1. What is Hardware looping? Mention advantages of it.
- 2. Write about Interrupts, Stacks.
- 3. Briefly explain Pipelining and Pipeline Depth.
- 11. Explain Interlocking.

12. Write about Branching effects, interrupt effects in processors.

#### UNIT –IV

1. Draw the architecture of TMSC54XX DSP and explain each block clearly.

2. Explain in detail the different instructions of TMSC54XX processor.

4. Briefly explain on-chip peripherals provided on TMS320C54XX processor.

5. Explain the following data addressing modes: a) Immediate addressing b) Absolute addressing c) Direct addressing.

6. Explain about indirect addressing with neat block diagram

7. Explain memory space of TMS320C54XX processor.

8. Explain about program control unit of TMS320C54XX processor.

9. Write a program to implement FIR filters.

#### UNIT –V

1. Draw the butterfly diagram for 2, 4, and 8 points using DITFFT.

2.Write a program to implement an 8-point DITFFT algorithm.

3. Explain the implementation procedure of interpolation operation.

4. a) what is Q-notation? Why it is used?

b) Represent 4400h as Q7,Q15 notation.

Explain CODEC interface unit with neat diagram.

5. Explain about parallel and memory I/O interfaces.

6. Explain about External bus interfacing I/O interface.

7. Write notes on MCBSP

8. Explain direct memory access in detail.

# (13EC431B) EMBEDDED SYSTEMS

#### **Course Description:**

This course provides an introduction to Embedded Systems with required hardware and software units. Issues such as embedded processor selection, Embedded SoC and use of VLSI Circuit Design Technology will be discussed. Embedded system design process will be discussed. The Intel 8051, a very popular microcontroller, will be studied. The architecture and instruction set of the microcontroller will be discussed. Memory structure, register structure, instruction set, external interfaces, modes of operation, assembly language programming and introduces architectural concepts and programming of 8051 microcontroller. Programmable system on chip with digital blocks and analog blocks will be discussed. This course covers Embedded / RTOS Concepts and Embedded Software Development Tools. ARM, SHARC processors concepts will be discussed in this course. This course provides information about advanced buses like I2C and CAN

#### Prerequisites

Fundamentals of computer architecture and requires the knowledge of MICROPROCESSORS & MICROCONTROLLERS

#### **Course Objectives**

- 1. Explains the design issues of embedded systems.
- 2. Comprehend architecture and programming of 8051 controller.
- 3. Interprets PSoC concepts
- 4. Interprets the basics of real-time operating system.
- 5. Impart the embedded basics of RTOS compliers, assemblers, Linker/Locators and debugging technique

#### **COURSE OUTCOMES:**

The students will be able to

- 1. Interprets embedded system basic concepts and designing.
- 2. Explains the programming model and basic features of a microcontroller.
- 3. Distinguishes s assembly language programming concepts of a microcontroller
- 4. Develop analog and digital applications using PSoC
- 5. Comprehends the architecture of the kernel of an operating system, details of task scheduling algorithms, knowledge of inter-task communication and other embedded RTOS concepts.
- 6. Comprehends the embedded software development tools.

- 7. Explains instruction set and programming model of ARM and SHARC processors
- 8. Describes bus protocols for embedded systems

## SYLLABUS

#### UNIT – I

**Embedded Computing:** Introduction, processor Embedded into a system, hardware units, software units in a system, Embedded SoC and use of VLSI Circuit Design Technology, Embedded System Design Process.

#### UNIT – II

**8051** Architecture and Programming: Introduction, 8051 Microcontroller Hardware, Timers and Counters, I/O Ports and Circuits, Serial Data Communication, External Memory, Interrupts.

Assembly Language Programming Process, 8051 Instruction Set: Data Transfer, Arithmetic, Logical and Branch Instructions, Decimal Arithmetic, Interrupt Programming.

#### UNIT – III

**Psoc Architecture and Programming:** PSoC as a Single-Chip Solution for Embedded System Design, Analog, Digital and Controller (8051) Blocks in PSoC, Hardware Programming through PSoC Creator, I/O Pin Configurability and applications.

#### UNIT – IV

**Embedded / RTOS Concepts:** Architecture of the Kernel, Tasks and Task scheduler, Interrupt service routines, Semaphores, Mutex, Mailboxes, Message Queues, Event Registers, Pipes, Signals, Timers, Memory Management, Priority inversion problem, Embedded operating systems, Embedded Linux, Real-time operating systems, RT Linux

**Embedded Software Development Tools**: Host and Target machines, Linker/Locators for Embedded Software, Getting Embedded Software into the Target System, Debugging Techniques

## UNIT – V

**Introduction to Advanced Architectures:** ARM and SHARC, Processor and memory organization and Instruction level parallelism, Networked embedded systems: Bus protocols, I2C bus and CAN bus, Internet – Enabled Systems, Design Examples – Elevator Controller.

#### **TEXT BOOKS:**

- 1. Raj Kamal, "Introduction to Embedded Systems", TMS, 2002
- Wayne Wolf, "Computers as Components Principles of Embedded Computing System Design" Elsevier (2<sup>nd</sup> Edition). ISBN-13: 9781558605411
- 3. Kenneth J. Ayala ,"8051 Microcontroller", Penram International.
- 4. David E. Simon, "An Embedded Software Primer "Pearson Education

#### **REFERENCE BOOKS:**

 Muhammad Ali Mazidi, "The 8051 Microcontroller and Embedded System", Pearson, 2<sup>nd</sup> Ed. ISBN: 9788131710265

- 2. Sri Ram V Iyer, Pankaj Gupta, "Embedded Real Time Systems Programming", TMH, 2004. ISBN:0-07-048284-5
- 3. Shibu K.V "Introduction to Embedded Systems", Mc Graw Hill

#### WEBSITES

- 1. books.askvenkat.com/2015/08/embedded-systems-textbook-by-rajkamal.html
- 2. books.google.co.in
- 3. www.psoc.com
- 4. www.cypress.com
- 5. Sharc.com
- 6. home.iitj.ac.in
- 7. unex.uci.edu
- 8. en.wikibooks.org/wiki/Embedded\_Systems
- 9. www.edgefx.in

#### **CONTENT BEYOND SYLLABUS:**

Embedded systems design

# LECTURE PLAN

Sl. No.	Topics in syllabus	Modules and Sub modules	Lecture No.	Suggested books with Page Nos.
UNIT	$\Gamma - I$ (No. of Lectures – 9)			
1	Introduction to Embedded systems	Introduction to Embedded systems	L1	T1, <b>3-5</b>
2	processor Embedded into a system	processor Embedded into a system	L2 L3	T1, <b>5-10</b>
3	hardware units	hardware units	L4 L5	T1, <b>10-18</b>
4	software units in a system	software units in a system	L6 L7	T1, <b>19-27</b>
5	Embedded SoC, VLSI Circuit Design Technology	Embedded SoC, VLSI Circuit Design Technology	L8	T1, <b>29-31</b>
6	Embedded System Design Process	Embedded System Design Process	L9	T1, <b>37-44</b>
	<b>T-II(No.of Lectures – 16)</b>			
7	Introduction to microcontrollers, hardware	Introduction, features, microcontroller hardware	L10 L11	R1, <b>23-31</b>
8	Basic assembly language programming process	Basic assemblylanguageprogrammingprocess,Addressing Modes	L12	R1, <b>37-63</b>
9	Instruction set: Data transfer instructions	Data transfer instructions	L13 L14	R1, <b>15-</b>
10	Arithmetic operations, Decimal Arithmetic	Arithmetic operations, Decimal Arithmetic	L15 L16	R1, <b>140-154</b>
11	Logical instructions	Logical instructions	L17	R1, <b>155-166</b>
12	Branch instructions	Branch instructions	L18 L19	R1, <b>70-80</b>
13	counters and timers	T0,T1,TMOD,TCON	L20 L21	R1, <b>240-260</b>
14	External memory	External memory	L22	R1, <b>412-443</b>
15	Serial data input and output	Serial data input and output	L23	R1, <b>278-298</b>
16	Interrupts and I/O programming	IP,IE,IO ports, programming	L24 L25	R1, <b>318-340</b> 94-106
UNIT	<b>[-III(No.of Lectures – 6)</b>			
17	PSoC Architecture	Introduction, PSoC Architecture	L26 L27	
18	Digital blocks in PSoC	Digital blocks in PSoC	L28	W3 & W4
19	Analog Blocks in PSoC	Analog Blocks in PSoC	L29	

	Hardware Programming	Hardwara Programming		
20	6 6	Hardware Programming	L30	
20	through PSoC Creator, I/O	through PSoC Creator, I/O	L30	
21	Pin Configurability	Pin Configurability	T 21	-
21	Applications	Applications	L31	
UNI	<b>I-IV(No.of Lectures -10)</b>	Introduction Architecture of		
22	Architecture of the Kernel	Introduction, Architecture of the Kernel	L32	T1, <b>350-354</b>
23	Tasks and Task scheduler, Interrupt service routines	Tasks and Task scheduler, Interrupt service routines	L33	T4, <b>164-173</b> <b>219-226</b>
24	· ·	Semaphores, mutex	L34	T4, <b>173-188</b>
24	Semaphores, mutex	1 .	L34	14, 1/3-100
25	Mailboxes, Message Queues, Event Registers, Pipes	Mailboxes , Message Queues, Event Registers, Pipes	L35	T4, <b>193-204</b>
26	Signals, Timers, Memory Management, Priority inversion problem	Signals, Timers, Memory Management, Priority inversion problem	L36	T4, <b>204-219</b>
27	Embedded operating systems :Embedded Linux, Real-time operating systems	Embedded operating systems :Embedded Linux, Real-time operating systems	L37	T1, <b>496-505</b>
28	EmbeddedSoftwareDevelopmentTools:Hostand Target machines	Host and Target machines	L38	T4, <b>281-283</b>
29	Linker/Locators for Embedded Software	Linker/Locators for Embedded Software	L39	T4, <b>283-296</b>
30	Getting Embedded Software into the Target System	Getting Embedded Software into the Target System	L40	T4, <b>296-300</b>
31	Debugging Techniques	Debugging Techniques	L41 L42	T4, <b>303-346</b>
UNI	<b>Γ-V(No.of Lectures -11)</b>			
32	ARM processor, features	Introduction, ARM processor, features	L43	
33	memory organization	memory organization, Addressing modes	L44	T2, <b>59-75</b>
34	Instruction set	Data processing Data transfer control instructions	L45 L46 L47	
35	SHARC processor and memory organization	SHARC processor and memory organization	L48	
36	Data operations	Data operations	L49 L50	W5
37	Instruction level parallelism	Instruction level parallelism	L51	
40	Network embedded systems: Bus protocols: I2C	Network embedded systems: Bus protocols: I2C	L52	T2, <b>405-406</b>
41	CAN bus	CAN bus	L53	T1, <b>161</b>
42	Internet enabled systems	Internet enabled systems	L54	T2, <b>416</b>
43	Design examples	Design examples	L55	T2, <b>427</b>
44	Design examples	Design examples	L56	T2, <b>427</b>
45	Revision	Revision	L57	,
46	Revision	Revision	L58	
47	Revision	Revision	L59	
48	Revision	Revision	L60	
.0			200	1

#### **Review Questions**

#### UNIT-I

- 1. Define embedded system
- 2. What is an embedded computing system?
- 3. Distinguish between microprocessor and microcontroller.
- 4. What are the common structure units in most processor?
- 5. What is a co-processor?
- 6. Mention various software units of Embedded System.
- 7. Explain embedded hardware units and devices in a system.
- 8. Explain Embedded System-On-Chip (SOC) and use of VSLI circuit design technology.
- 9. Draw the ES design and development life cycle model and briefly explain.
- 10. Explain various characteristics required in the selection of a processor to design an ES with suitable examples.
- 11. What are the design issues in ES?
- 12. Explain the important problems/challenges that must be considered while designing embedded systems?
- 13. Explain examples of embedded system.

#### UNIT-II

- 1. Distinguish between DPTR and PC.
- 2. What is special function registers?
- 3. Explain CALL and Return
- 4. Give the formats of TMOD, TCON. PCON, IE, IP, SCON, PSW.
- 5. Explain Logical and Branch Instructions.
- 6. Explain 8051 oscillator and clock.
- 7. Differentiate between MOVX & MOVC instructions of 8051?
- 8. Write about register banks in 8051.
- 9. Describe various addressing modes of 8051.
- 10. Describe function of pins of 8051 microcontroller.
- 11. Explain 8051 architectural features. What are the devices internally present in the classic 8051?
- 12. Describe various modes of timer of 8051 microcontroller.

- 13. Describe interrupt structure of 8051.
- 14. Draw the memory organization in 8051.
- 15. Interface external program memory with 8051 & explain how the data is transferred and draw timing diagram for reading external ROM.
- 16. Write a program to multiply the unsigned number in register R3 by the unsigned number on port 2 and put the result in external RAM locations 10H (MSB) & 11H (LSB).
- 17. Write an ALP to generate a square wave of 12 kHz using 8051 MC (CF = 12 MHz).
- 18. Write ALP in 8051 prepare a look up table that converts HEX number in A (O-F) to its ASCII equivalent.
- 19. Write an ALP in 8051 to find maximum number from the set of n numbers.

#### UNIT-III

- 1. What is meant by dynamic reconfiguration of PSoC?
- 2. Explain the analog block topology of PSoC.
- 3. Describe about digital blocks in PSoC
- 4. Explain the process of serial communication carried out using PSoC.
- 5. Explain I/O pin configurability and application.
- 6. What do you mean by SOC?
- 7. Explain a single-chip solution for Embedded System Design.
- 8. Draw the architecture of PSoC and explain main subsystems.

#### **UNIT-IV**

- 1. Distinguish between process, task, and thread?
- 2. Mention three methods of protecting shared data with examples
- 3. What are the OS functions at an RTOS kernel?
- 4. What is semaphore?
- 5. What is the use of target system in ES development?
- 6. Explain the use of various software tools in ES development.
- 7. With a suitable example explain the basic method of testing embedded software on the development host with a suitable example.
- 8. Describe Task management and synchronization of RT linux.
- 9. Explain the methods of handling interrupt service in RTOs.
- 10. Write short notes on Architecture of kernel and RTOS scheduling algorithms.

- 11. What is TCB in RTOS?
- 12. Explain software-only-monitor.
- 13. Explain briefly about timer functions and other timing services.
- 14. Explain the term MUTEX.
- 15. Explain different methods of getting software into a target system.
- 16. Define the term CODEC.
- 17. Define Embedded Linux.
- 18. Define Debugging technique.
- 19. Explain functions of device programmer.
- 20. Explain the needs for memory management in RTOS.
- 21. What is meant by a pipe? How does a pipe may differ from a queue.
- 22. Distinguish between Embedded Linux and Real time Linux.
- 23. How do you solve priority Inversion problems?
- 24. Discuss Linker/Locator for embedded software.
- 25. Discuss about different Debugging tools.
- 26. What do you mean by 'real time' and 'real time clock'?
- 27. Why do you need at least one timer device in embedded systems?
- 28. How pipe is different from Message Queue?
- 29. Explain hard real-time scheduling and soft real-time scheduling considerations?
- 30. Distinguish between emulators and simulators?

#### UNIT-V

- 1. What are the data types supported by SHARC processor
- 2. Explain the architectural features of SHARC and how the instruction level parallelism is implemented.
- 3. Explain the features and functions of 12C and CAN bus.
- 4. Write short notes on ARM address translation
- 5. How is the context switching handled in ARM processors?
- 6. Explain network embedded system.
- 7. Discuss the data operations of ARM processor.

- 8. Explain instruction level parallelism.
- 9. Explain the design example of elevator controller.
- 10. Explain memory organization and programming model of ARM processor.
- 11. What are net enabled embedded system?
- 12. Give two bus protocols that can be implemented on an ARM processor?
- 13. Give I2C protocol?
- 14. Explain arithmetic & logical instructions in ARM processor.

#### (13EC430) COMPUTER NETWORKS

#### **Course Description:**

A computer network or data network is a telecommunications network which allows computers to exchange data. In computer networks, networked computing devices exchange data with each other using a data link. The connections between nodes are established using either cable media or wireless media. The best-known computer network is the Internet.

Network computer devices that originate, route and terminate the data are called network nodes. Nodes can include hosts such as personal computers, phones, servers as well as networking hardware. Two such devices can be said to be networked together when one device is able to exchange information with the other device, whether or not they have a direct connection to each other.

Computer networks differ in the transmission medium used to carry their signals, the communications protocols to organize network traffic, the network's size, topology and organizational intent.

Computer networks support an enormous number of applications such as access to the World Wide Web, video, digital audio, shared use of application and storage servers, printers, and fax machines, and use of email and instant messaging applications as well as many others. In most cases, application-specific communications protocols are layered (i.e. carried as payload) over other more general communications protocols.

#### Prerequisites

Requires the knowledge of communication, fundamentals of computer.

#### **COURSE OBJECTIVES :**

- 1. Define different network topologies and network models.
- 2. Explain the functions of Physical layer in OSI model.
- 3. Discuss the functions of Data link layer in OSI model.
- 4. Classify the routing algorithms and the functions of various networks.
- 5. Illustrate the protocols used in Transport layer and different applications in application layer.

#### **COURSE OUTCOMES:**

The students will be able to

- 1. Describe the architecture of computer communication networks
- 2. Distinguish various topologies.
- 3. Design protocols for various layers
- 4. Apply different protocols in various layers

- 5. Apply error detection and correction methods in data link layer.
- 6. Understand wireless networks
- 7. Apply different algorithms for congestion control and quality of service
- 8. Develop different applications using protocols.

#### UNIT – I

Introduction to networks, internet, protocols and standards, the OSI model, layers in OSI model, TCP/IP suite, Addressing.

#### UNIT – II

**Physical Layer:** Digital transmission, multiplexing, transmission media, circuit switched networks, datagram networks, virtual circuit networks.

#### UNIT – III

**Data link Layer:** Introduction, Block Coding, cyclic codes, checksum, framing, flow and error control, Noiseless channels, noisy channels, HDLC, point to point protocols.

Medium Access sub layer: Random access, controlled access, channelization, IEEE standards, Ethernet, Fast Ethernet. Giga-Bit Ethernet, wireless LANs.

#### UNIT – IV

**Connecting LANs:** backbone networks and virtual LANs, Wireless WANs SONET, frame relay and ATM. Network Layer: Logical addressing, internetworking, tunneling, address mapping, ICMP, IGMP, forwarding, uni-cast routing protocols, multicast routing protocols.

#### $\mathbf{UNIT} - \mathbf{V}$

**Transport Layer:** Process to process delivery, UDP and TCP protocols, SCTP, data traffic, congestion, congestion control, QoS, integrated services differentiated services, QoS in switched networks. Application Layer – Domain name space, DNS in internet, electronic mail, FTP, WWW. HTTP, SNMP, multi-media.

#### **TEXT BOOKS:**

- 1. Andrew S Tanenbaum, "Computer Networks", 4<sup>th</sup> Edition, Pearson Education. *ISBN*: 9780130661029
- 2. Behrouz A. Forouzan, "Data Communications and Networking", Fourth Edition, TMH 2006. *ISBN* 978-0-07-296775-3 *ISBN* 0-07-296775-7

#### **REFERENCE BOOKS:**

- 1. W.A. Shay, "Understanding communications and Networks", 3<sup>rd</sup> Edition, Cengage Learning
- 2. Nader F. Mir, "Computer and Communication Networks", Pearson education. *ISBN*, 0132797151, 9780132797153

#### WEBSITES

- 9. http://nptel.ac.in/courses/106105081/1
- 10. <u>http://ecourses.vtu.ac.in/nptel/courses/Webcourseconten</u>IIT-MADRAS/ComputerNetworks/pdf/
- 11. www.cse.iitk.ac.in/users/dheeraj/cs425/
- 12. www.mhhe.com/engcs/compsci/forouzan/

- 13. iit.qau.edu.pk
- 14. http://accessengineeringlibrary.com/browse/data-communications-and-networking-fourth-edition
- 15. https://www.smartzworld.com/notes/computer-network-cn/
- 16. http://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-829computer-networks-fall-2002/lecture-notes/

#### **CONTENT BEYOND SYLLABUS:**

- 1. Techniques to improve Quality of Service(QOS).
- 2. Active and Fair Queue Management Schemes.
- 3. Bluetooth Technology with protocol stack.
- 4. cellular systems.
- 5. Virtual private Networks
- 6. Wi-Max

## **LECTURE PLAN**

Sl. No.	Topics in syllabus	Modules and Sub modules	Lecture No.	Suggested books with Page Nos.
UNII	<b>T – I</b> (No. of Lectures	- 10)		
1	Introduction to Networks	Physical structures Network models	L1 L2	Forouzan-7 Forouzan-13
2	internet	Brief history and internet today	L3	Forouzan-16
3	protocols and standards	protocols and standards Standard organization	L4	Forouzan-19
4	OSI model	Layered architecture,Peer-to-peer process	L5	Forouzan-29
5	layers in OSI model	Physical layer,Data link layer Network layer, Transport layer Session,presentation,application layers	L6 L7	Forouzan-33
6	TCP/IP suite	Physical layer,Data link layer Network layer, Transport layer ,application layers	L8	Forouzan-42
7	Addressing	Physical address, logical address Port address, specific address	L9	Forouzan-45
8	Analog and digital signals	Analog and digital signals Periodic and non-periodic signals	L10	Forouzan-57
UNIT	<b>I –II</b> (No. of Lectures	5 – 16)		1
9	Introduction to Physical Layer	Introduction to Physical Layer	L11	Forouzan-55
10	Digital transmission	Digital to digital transmission Analog to Digital conversion Transmission modes	L12 L13 L14	Forouzan-71
11	multiplexing	FDM WDM STDM	L15 L16 L17	Forouzan-161
12	transmission media	Guided media Unguided media(wireless)	L18 L19	Forouzan-192
13	circuit switched networks	Three phases Circuit switched technology in telephone networks	L20 L21	Forouzan-214
14	Datagram networks	Routing table Datagram networks in the internet	L22	Forouzan-218
15	virtual circuit networks	Addressing, three phases efficiency. virtual circuit networks in WAN	L23 L24	Forouzan-221
16	Switch and	Major components,	L25	Forouzan-241

	telephone network	LATA, signaling	L26	
UNIT	Г–III (No. of Lecture	es – 23)		
17	<b>Data link Layer:</b> Introduction,	Types of errors, Redundancy, detection Vs correction FEC	L27	Forouzan-267
18	Block Coding	Error detection error correction hamming distance	L28 L29	Forouzan-271
19	cyclic codes	Cyclic redundancy check	L30	Forouzan-284
20	checksum, framing	Ones complement, Internet check sum	L31	Forouzan-298
21	flow and error controlin Noiseless channels	Simplest and stop and wait protocol	L32	Forouzan-312
22	noisy channels	Stop and wait ARQ Go back N ARQ Selective repeat ARQ	L33 L34 L35	Forouzan-318
23	HDLC	Configuration and transfer mode Frames,control field	L36	Forouzan-340
24	point to point protocols	Framing Transition phases	L37	Forouzan-346
25	Medium Access sub layer: Random access	ALOHA CSMA,CSMA/CD,CSMA/CA	L38 L39 L40	Forouzan-364
26	wireless LANs	IEEE 802.11 Bluetooth	L41 L42	Forouzan-395
27	controlled access	Reservation Polling Token passing	L43	Forouzan-379
28	channelization	FDMA TDMA CDMA	L44 L45 L46	Forouzan-383
29	IEEE standards, Ethernet	MAC Layer, physical layer	L47	Forouzan-397
30	Fast Ethernet	MAC Layer, physical layer	L48	Forouzan-409
31	Giga-Bit Ethernet	MAC Layer, physical layer	L49	Forouzan-412
UNIT	Γ – IV (No. of Lecture	es – 12)		
32	Connecting LANs	Connecting devices	L50	Forouzan-445
33	backbone networks and virtual LANs	Bus back bone, star back bone	L51	Forouzan-456
34	Wireless WANs	Cellular telephony, Satellite	L52	Forouzan-467

		networks		
35	SONET	Architecture,SONET layers SONET Frame format,STS multiplexing	L53	Forouzan-478
36	frame relay and ATM	Architecture Frame relay layers ATM architecture ATM layers	L54	Forouzan-517
37	Network Layer: Logical addressing	IPv4 address IP v6 Address	L55	Forouzan-523
38	internetworking	Need for network layer Internet as datagram network	L56	Forouzan-579
39	Address mapping, ICMP, IGMP, forwarding	ARP,RARP Message format of ICMP Message format of IGMP Forwarding techniques	L57 L58	Forouzan-612
40	Uni-cast routing protocols	DSR LSR PVR	L59 L60	Forouzan-658
41	multicast routing protocols	Multicast Protocols	L61	Forouzan-678
UNIT	Γ-V (No. of Lectures	- 08)		
42	<b>Transport Layer:</b> Process to process delivery UDP protocols	Client server paradigm Multiplexing and de-multiplexing Frame format UDP	L62	Forouzan-703 Forouzan-709
43	TCP protocols	Frame format of TCP	L63	Forouzan-715
44	SCTP	SCTP services, features and frame format.	L64	Forouzan-736
45	Congestion, congestion control,QOS	Openloop and closed loop congestion control, Technique to improve QOS	L65	Forouzan- 765 Forouzan-775
46	Integrated services,differentiat ed services.	Signaling, flow specification DS Field	L66	Forouzan-780
47	Application Layer	Domain name space, DNS in internet, electronic mail, FTP, WWW, HTTP, SNMP, Multi-media.	L67 L68 L69	Forouzan-801 Forouzan-824 Forouzan-840 Forouzan-851 Forouzan-861

## Review Questions UNIT 1 PART A

1. Define Networks.

2. Define Internetworking and Intranetworking.

- 3. What are Unicast, Multicast, and Broadcast?
- 4. What is Multiplexing and Demultiplexing?
- 5. What is Synchronous Time Division Multiplexing?
- 6. What is Frequency Division Multiplexing?
- 7. What is Statistical Multiplexing?
- 8. What are LAN, WAN and MAN?
- 9. Define Bandwidth and Latency
- 10. Define Data communication
- 11. With the example define half duplex communication.
- 12. Name four topologies of computer networks.
- 13. Define OSI model and what are the seven layers of OSI Model?
- 14. Define Line coding
- 15. Different types of encoding

### PART B

- 1. Explain about OSI Architecture with neat sketch on it.
- 2. What is meant by topology? and explain the topologies of the network.
- 3. Explain the categories of networks.

#### UNIT 2 PART-A

- 1. What is a virtual circuit?
- 2. What are data grams?
- 3. What are the two types of implementation formats in virtual circuits?
- 4. What are Switching and Bridging?
- 5. What is Virtual Circuit Switching?
- 6. Explain line coding (digital to digital conversion).
- 7. What is frame & framing bits?
- 8. What is interleaving?

### PART B

- 1.Explainabou different types of multiplexing,
- 2. Classify transmission media and explain about them
- 3.Explain circuit switched networks
- 4.Explain datagram networks,
- 5.Explain virtual circuit networks.

# UNIT 3

## PART A

- 1. What is repeater?
- 2. What is Media Access Control?
- 3. What is Exponential backoff?
- 4. What is Orthogonal Frequency Division Multiplexing?
- 5. Define Signal to Noise Ratio.
- 6. What is Access Point?
- 7. What is Bluetooth?
- 8. What is Piconet?
- 9. What are the responsibilities of data link layer?
- 10. Mention the types of errors.
- 11. What is redundancy?
- 12. List out the available detection methods.
- .13. Define checksum.
- 14. Write short notes on error correction.
- 15. Mention the types of error correcting methods.
- 16. What is the purpose of hamming code?
- 17. Mention the categories of flow control.
- 18. What is the function of stop and wait flow control?
- 19. Mention the advantage and disadvantage of stop and wait flow control.
- 20. Define ARQ.
- 21. Mention the function of go-back N-ARQ.
- 22. What is selective reject ARQ?
- 23. Define HDLC.
- 24.List the types of stations is HDLC.
- 25. What are the different communication modes in HDLC?
- 26. Mention the types of frames in HDLC.
- 26. What is meant by bit stuffing?
- 27. What is meant by LAN and Mention the various architecture in a LAN?
- 28. Define a standard 802.3
- 29. What is piggy backing?

### PART B

- 1. Explain about Ethernet (802.3).
- 2. Explain about Wi-Fi (802.11).
- 3. Explain about Bluetooth with its architecture.
- 4. Explain about Switching and Bridging.
- 5. Explain error detection and error correction techniques.
- 6. Explain error control mechanism.
- 7. Explain the flow control mechanism
- 8. Explain the timers and time registers in FDDI.
- 9. Explain about Ethernet.
- 10. Explain about HDLC.

### UNIT 4 PART A

- 1. Difference between Forwarding and Routing.
- 2. What is Interior Gateway Protocol (IGP)?
- 3. List the two different classes of routing protocol.
- 4. What is distance vector routing?
- 5. What is Count to infinity problem?
- 6. What is RIP?
- 7. What is Link State Routing?
- 8. Draw the sketch of OSPF header format.
- 9. Difference between IPv4 and IPv6.
- 10. Draw the sketch of IPv6 Packet Header.
- 11. What is Network Address Translation?
- 12. What is Multicast?
- 13. What is Switching?
- 14. What are the responsibilities of network layer?
- 15. What is meant by switched & permanent virtual circuit?
- 16. Define Routers.
- 17. What is meant by hop count?
- 18. How can the routing be classified?
- 19. Write the keys for understanding the distance vector & link state routing.
- 20. How the packet cost referred in distance vector and link state routing?
- 21. How the routers get the information about neighbor?
- 22. What are the four internetworking devices?
- 23. Define IP address.
- 24. Define Gateway.
- 25. What is LSP?
- 26. Define Subnetting.
- 27. Define Masking.

### PART B

- 1. Explain about Switching and Forwarding.
- 2. Explain about RIP.
- 3. Explain about OSPF.
- 4. Explain about BGP.
- 5. Explain about Routing areas.
- 6. Explain about IPv6.
- 7. Explain about Multicast.
- 8. Explain about Multicast address
- 9. Explain the two approaches of packet switching techniques.
- 10. Explain IP addressing method.
- 11. Define routing & explain distance vector routing and link state routing.
- 12. Define Routers and explain the type of routers.
- 13. Explain sub netting
- 14. Write short notes about repeaters, routers and gateways.

#### UNIT 5 PART A

- 1. What is function of transport layer?
- 2. What are the duties of the transport layer?
- 3. What is the difference between network layer delivery and the transport layer delivery?
- 4. What are the four aspects related to the reliable delivery of data?

- 5. What is meant by segment?
- 6. What are the two possible transport services?

7. The transport layer creates the connection between source and destination. 8. What are the three events involved in the connection?

- 9. What are the techniques used in multiplexing?
- 10. What is meant by congestion?
- 11. Why the congestion occur in network?
- 12. How will the congestion be avoided?
- 13. What is the function of BECN BIT?
- 14. What is the function of FECN?
- 15. What is meant by quality of service?
- 16. What are the two categories of QOS attributes?
- 17. What is SMTP?
- 18. What is HTTP?
- 19. What is DNS?
- 20. What is SNMP?
- 21. What is URL?

### PART B

- 1. Explain the duties of transport layer.
- 2. Explain UDP & TCP.
- 3. Explain about congestion control.
- 4. Explain leaky bucket and token bucket algorithm
- 5. Explain the functions of SMTP.
- 6. Write short notes on FTP.
- 7. Explain about HTTP.
- 8.. Explain the WWW in detail.
- 9. Explain about the operation of TCP with neat sketch on it.
- 10. Explain about the concept of sliding window protocol.
- 11. Explain about UDP with neat sketch on it.
- 12. (i). Difference between UDP and TCP.
- (ii). Discuss flow control with an example.
- 13. Explain about the three way handshake protocol for connection establishment in TCP.
- 14. Explain about the TCP congestion control.
- 15. Explain about the RED algorithm.
- 16. Explain about the concept of congestion avoidance in TCP?
- 17. Explain about the RSVP protocol with neat sketch.
- 18. Explain about the differentiated services.

### Assignment-I

- 1.Explain different types of Ethernets.
- 2.Explain about flow and error control methods
- 3. Explain about circuit, packet, data gram switching networks
- 4.Explain sliding window protocols
- 5.Explainabout HDLC Protocol

#### Assignment-II

- 1.Explain about TCP protocol
- 2.Explain about UDP Protocol

- 3.Explain unicast routing protocols4.Explain about multicast routing protocols5.ExplainFTP,WWW,e-mail

### (13EC429) ELECTRONIC MEASUREMENT AND INSTRUMENTATION

### **Course Description:**

This is a course that deals with the basic working of instruments used for measurement. The course then covers different electrical measuring instruments like Ammeters, Voltmeters, Energy meters, Bridges, Potentiometers It also introduces various measurement techniques available, errors in measurements and their rectification. It also deals with various types of signal generators, oscilloscopes, Transducers

Pre-requisite: Linear Integrated Circuits

### **COURSE OBJECTIVES:**

- 1. To learn the performance characteristics of electronic instruments.
- 2. To learn various measuring instruments.
- 3. To learn various bridges and signal analyzer instruments.
- 4. To learn electronic instruments like CRO and its applications.
- 5. To learn various transducers and their classification.

## **COURSE OUTCOMES:**

The students will be able to

- 1. Demonstrate various electronic instruments and their utilization.
- 2. Analyze the Performance characteristics of each instrument
- 3. Design basic meters in engineering.
- 4. Understanding about different types of signal Analyzers in engineering
- 5. Understanding the basic features of oscilloscope and its internal structures and different types of oscilloscopes
- 6. Analyze various transducers and their applications in engineering.
- understanding how different physical parameters like pressure, force, velocity etc. are measured
- 8. Develop the complete knowledge of various electronics instruments used in the field of engineering and technology.

### UNIT – I

**Electronic Measurements:** Significance of Measurement & block diagram of Measurement System, Static characteristics- Accuracy, Precision, Sensitivity, Linearity, Repeatability,

Reproducibility, Resolution, Threshold, Drift , Stability, Dynamic Characteristics- speed of response, measuring lag, fidelity, dynamic error, Types of Errors.

## UNIT -II

**Measuring instrument**: PMMC, DC voltmeter and current meters and its Extension ranges, True RMS Responding Voltmeter, Average response rectifier type, electronic voltmeter, block diagram approach for measurement of voltage, current and Resistance using Digital Multi Meter (DMM) – Basic Potentiometer Circuit – Q-meter.

## UNIT – III

**Bridges and Analyzers:** resistance measurement using substitution, ammeter method, voltmeter method, DC Bridge- Wheatstone bridge, Kelvin's Double Bridge, AC Bridge-Maxwell's Bridge, Schering bridge and Wien's Bridge.

**Signal analyzers:**, **Frequency** Selective & Heterodyne Wave Analyzers, Spectrum Analyzers, Harmonic distortion Analyzers, Total Harmonic distortion.

## $\mathbf{UNIT} - \mathbf{IV}$

**Oscilloscopes:** Cathode Ray Tube (CRT), Electrostatic Deflection, Post Deflection and Acceleration of Electron Beam, Screens for CRT's, Block diagram of CRO, Time-Base Generator, Free running and Triggered Sweeps, Attenuators– Digital Storage Oscilloscope – Applications of CRO: Measurement of Phase and Frequency using Lissajous Patterns.

## UNIT – V

**Transducers:** Transducer and its classification, ideal Requirements of Transducer – Resistive Transducer: Potentiometric type, Strain Gauge type (Gauge factor derivation, SG materials, Bonded and unbounded strain gauges), Capacitive Transducers - Variable gap type, variable area type & variable Dielectric type, Inductive Transducers - LVDT, RTD, Thermocouple, Piezo Electric Transducers (Piezoelectric effect, Piezoelectric materials, frequency response of PZT).

## TEXT BOOKS

- 1. Sawhney A. K., A Course in Electrical and Electronics Measurements and Instrumentation, Dhanpat Rai and Sons, New Delhi, 1995.
- 2. Kalsi.H.S., Electronic Instrumentation, 2002.
- 3. Cooper W.D & Hlefrick A.D., Electronic Instrumentation & Measurement Technique, III Edition, Prentice Hall of India 1991.

## **REFERENCE BOOKS**

- 1. Rajendraprasad, Electrical Measurements and Measuring Instruments, Khanna Publishers, New Delhi, 1999.
- 2. Gupta J.B, Electrical Measurements and Measuring Instruments, S.K. Kataria & Sons, New Delhi, 1993. 3. B.M. Oliver and J.M.Gage, Electronic Measurements and Instrumentation, McGraw Hill 1977.

## WEBSITES

17. http://web.mit.edu/2.671/www/ebooks.cambridge.org

18. nptel.ac.in

**CONTENT BEYOND SYLLABUS:** 

1. Applications of different measuring instruments in industries.

## LECTURE PLAN

Sl. No.	Topics in syllabus	Modules and Sub modules	Lecture No.	Suggested books with Page Nos.
UNIT	$\Gamma - I$ (No. of Lectures	- 19)		
1	SignificanceofMeasurement&blockdiagramofMeasurementSystem,	Introduction to measurement and its significance	L1	1 TB1
2	block diagram of Measurement System,	Primary transducer ,data conversion, data manipulation blocks	L2 L3	3 TB1
3	Static characteristics	Accuracy,Precision,Sensitivity, Linearity,Repeatability, Reproducibility,Resolution,Thres hold, Drift ,Stability	L3 L4	24 TB1
4	Dynamic Characteristics	speed of response, measuring lag, fidelity,dynamic error	L5 L6	102 TB1
5	Types of errors	Absolute error, percentge of error, Environmentatl error,observational error,problems on errors	L7,L8	60 TB1
7	DC & AC Voltage measurements using Rectifier	Measurement of volatges using rectifier	L9,L10	80 TB3 135 TB3
8	electronic voltmeter	Introduction,	L11	740 TB3
9	Measurement of V,I,resistance using DigitalMulti Meter	Definition and advantage of digital meters over analog meters	L12 L13	27 TB2
10	Basic Potentiometer Circuit – Q-meter	Measurement of R, L,C using meter	L14 L15	951, 903 TB1
11	Bridge- Wheatstone bridge, Kelvin's Double Bridge	Basic balancing and unbalancing bridges	L16 L17	102 TB3
12	AC Bridge- Maxwell's Bridge, Schering bridge and Wien's Bridge.	Measurement of L ,C ,Problems on bridges	L18 L19	117 TB3

UNIT	- II (No.of Lectures -	14)		
13	Cathode Ray Tube (CRT),	Definition of CRT, blocks of CRT- type of cathode, deflection systems, post deflection and acceleration of beam, screen for CRTs.	L20 L21 L22	785 TB1
14	Block Diagram of CRO	Time base generator, triggered sweeps, delay, vertical and horizontal deflection, attenuators	L23 L24 L25	806 TB1
15	Digital storage oscilloscope	Introduction to digital oscilloscope	L26	828 TB1
16	Dual trace , dual beam, sampling oscilloscope	Introduction to sampling	L27 L28 L29	815,816 TB1
17	Application of CRO	Measurement of phase and frequency,Lissajous patterns	L30	810 TB1
UNIT	<b>[-III] (No. of Lectures</b>	5-6)		
18	Selective & Heterodyne Wave Analyzers,	Definition of analyzer	L31 L32	282 TB3
19	Spectrum Analyzers, Harmonic distortion Analyzers,	Frequency domain representation of signals, definition of distortion	L33 L34	291 TB3
20	Total Harmonic distortion.	Definition of total harmonic distortion	L35	286 TB3
21	Magnetic tape recoder	Introduction to recorders	L36	1317 TB1
UNI	Г–IV (No. of Lecture	<u>s - 14)</u>		
22	Transducers	Introduction to transducer, Classification of transducers	L37 L38	913 TB1
23	Resistive transducer	Strain guage types of strain guages, poetentiometric transducers ,problems on strain guage	L39 L40 L41 L42	950 TB1
24	Capacitive transducer	Variable gap, variable area, dilectric type	L43	1014 TB1
25	Inductive transducer	LVDT	L44 L45	1001 TB1
26	Thermocouple,RTD	Definiton of thermocouple and RTD	L46 L47	979 TB1
27	Piezo electric transducers	Piezoelectric effect, Piezoelectric materials, frequency response of PZT	L48 L49	1028 TB1
28	problems	Problems	L50	
UNIT	Г -V Transducer App	lications ( No. of lectures - 7)		

28	Force Measurement using loadcells & Strain gauge	Introduction to strain guage	L51	1331 TB1
29	Temperature Measurement using Thermistor & Thermocouple	Introduction to thermocouple and thermistor	L52 L53	356 TB3
30	Pressure Measurement using Pressure sensing elements	Introduction to pressure sensing elements	L54	918 TB1
31	Flow Measurement using Electro Magnetic Flow Meter		L55	1403 TB1
32	Ultrasonic level guage		L56	1411 TB1
33	Sound measurement		L57	1415 TB1

## **Review Questions**

## **Unit I: Electronic Measurement**

- 1.With neat sketch, discuss in detail about the working principle of PMMC? Also list out the source of errors in PMMC and how are they minimized?
- 2. With a neat block diagram, explain about the functional elements of a measurement system. Also list out the possible errors of any system.
  - b. With a neat diagram explain the principle and operation of thermistor.
- 3. explain static characteristics in detail
- 4. explain in detail about systematic and randome errors in measurement
- 5. explain accuracy and precision in detail
- 6. list out the major categories of error in detail?
- 7. explain the types of forces in measurement system?

## Unit II:

- 1. Describe the principle of operation of Q-meter. Explain how high impedance component is measured using Q-meter.
- 2.Draw the block diagram of DMM and explain how it is used to measure AC & DC voltage, current and resistance.
- 3. Discuss about the different types of errors that occur in a measuremen using DMM.
- 4.Show that the error in potentiometric transducer is on account of the nonlinearity effect produced by the output device.
- 5. explain true rms meter in detail
- 6. explain average responding meter in detail
- 7. explain potentimetric circuit in detail
- 8 explain dc ammeter in detail
- 9. explain extension ranges of ammeter and voltmeter in detail
- 10.explain DC voltmeter in detail
- 11. discuss electronic voltmeter in detail

## Unit III:

- 1. Explain how the performance of heterodyne wave analyzer is better than resonant wave analyzer?
- 2. What is the role of Active filter section in wave analyzer? Explain how RF waves can be analyzed using signal mixing concept?
- 3. Using schematic block diagram explain the operation of frequency selective and heterodyne wave analyzers. explain spectrum analyzer in detail?
- 4. Explain total harmonic distortion analyzer in detail?
- 5. Suggest a bridge circuit for measuring low Q coil and derive the necessary balance equations to determine the unknown component?
- 6. How the ratio of arm resistances are related in case of Kelvin's Double bridge circuit. Derive
- 7. an expression from bridge circuit to determine very low resistance?
- 8. explain RF anlayzer in detail?

## **Unit IV: OSCILLOSCOPES**

- 1. An electrically deflected CRT has final anode voltage of 200V and parallel deflecting plates 1.5cm long and 5 mm apart. If the screen is 50 cm from the centre of the deflecting plates.
- 2. Find the deflection sensitivity and Deflection factor of the tube
- 3. With neat block diagram, explain in detail about the working principle of Dual trace Oscilloscope? Distinguish between ALT mode and CHOP modes of operation?
- 4. Discuss in brief about the working principle of Digital Storage Oscilloscope.
- 5. Derive an expression for the Deflection Sensitivity of a CRO.
- 6. Explain measurement of phase using Lissajous Patterns in CRO
- 7. Explain CRT In detail?
- 8. Explain block diagram of CRO in detail
- 9. Explain time base generator in detail?
- 10. explain delays circuit used in CRO?
- 11. Discuss post deflection in detail?

## **Unit V: Transducers**

- 1. Define pressure? Explain how pressure is measured using elastic elements?
- 2. What is rosette? Explain how it measures load applied in different directions.
- 3.Classify flow. Explain how hot wire anemometer measure flow rate?
- 4. With a neat sketch give the operation of capacitive type microphone.
- 5, Explain ultrasonic level guage ?6. Explain electromagnetic flow meter?
- 7. Define LDR and explain it in detail?
- 8. Explain how displacement is measured using LVDT.
- 9.Define transducer. Give its classification with suitable examples.
- 10. "Sensitivity and linearity are two conflicting requirements w.r.t. potentiometers" explain.
- 11.Define gauge factor. Prove that the relationship G.F. = 1 + 2v.
- 12. Write short notes on photoelectric transducers.
- 13,Explain bonded and unbounded strain gauges.
- 14. Explain how linear characteristic can be achieved in a capacitive transducer which works on the principle of change in distance between two plates.
- 15.Define residual voltage. With a neat sketch explain the principle and operation of LVDT. Mention its advantages and disadvantages.
- 16 With a neat diagram explain the principle and operation of thermistor.
- 17 write short notes on thermocouple

### **Short Questions**

1. 10 x 2

- 1 Why Wheatstone bridge is not used for measurement of very low resistances and very high resistances?
- 2. Explain the difference between percentage error and probable error.
- 3. Name the materials used for display in CRT'S.
- 4. Draw the Lissajous pattern obtained when two sinusoidal voltages of equal frequency which are in phase are applied to CRO plates.
- 5. How do you estimate the distortion of a wave?
- 6. Define Gauge factor.
- 7. Define SPL?
- 8. Why piezoelectric transducers are not used for static input?
- 9. What is piezoresistive effect?
- 10. How cold junction compensation can be done in thermocouple?
- 11. How a PMMC of range (0-100mA) with an internal resistance of 20  $\Box$  can be converted to a voltmeter of a range (0-50V).
- 12. List and brief about the limitations of Q-meter?
- 13. Draw the characteristics of different strain gauge materials.
- 14. Name the device which collects secondary emission electrons in CRO.
- 15. A Lissajous Pattern on an oscilloscope is stationary and has 5 horizontal tangencies and 2 vertical tangencies. The frequency of horizontal input is 1000 Hz. Determine the frequency of vertical input.
- 16. Write the expression for total harmonic distortion (THD).
- 17. Classify different piezoelectric materials.
- 18. Draw the symbol of photo transistor.
- 19. What is thermister?
- 20. Name the device used for temperature compensation in strain gauge circuits.
- 21. screen for crts
- 22. define deflection sensitivity of CRT
- 23. define observational and parallax error
- 24. disadvantage of wheatstone bridge
- 25. define accuracy
- 26. define active and passive transducers
- 27. torque equation of PMMC
- 28. define fidelity
- 29.define types of cros
- 30. define LVDT And write down its advantages

### (13EC427) MICROWAVE ENGINEERING

#### **Course Description:**

The central theme of this course concerns the basic principles and applications of microwave devices and circuits. Microwave techniques have been increasingly adopted in such diverse applications as radio astronomy, long-distance communications, space navigation, radar systems, medical equipment, and missile electronic systems. As a result of the accelerating rate of growth of microwave technology in research and industry, students who are preparing themselves for, and electronics engineers who are working in, the microwave area are faced with the need to understand the theoretical and experimental design and analysis of microwave devices and circuits.

#### **Prerequisites:**

Electromagnetic Theory and Transmission Lines.

### **Course objectives:**

The course objectives are to enable the students to:

- 1. Recall TE or TM mode analysis in transmission lines.(Remember)
- 2. Discuss the fundamental of microwave components to make a microwave circuit and derive scattering matrix.(Understand)
- 3. Sketch the microwave solid state devices and vacuum tubes. (Apply)
- 4. Compare the performance of vacuum tubes, microwave solid state devices. (Analyze)
- 5. Understand measurement of microwave Power, Attenuation, Frequency, VSWR and Impedance using microwave bench.(Understand)

#### **Course outcomes:**

After completion of course student will be able to

- 1. Retrieve the history and importance of microwave frequencies(Remember)
- 2. Compare TE or TM transmission along waveguides(Analyze)
- 3. Describe the operation of various microwave components (Understand)
- 4. Apply scattering matrix to prove the properties of microwave passive devices. (Apply)
- 5. Explain the operation of microwave tubes and microwave solid state devices. (Understand)
- 6. Categorize microwave sources and amplifiers. (Analyze)
- 7. Recommend appropriate methods to measure microwave Power, Attenuation, Frequency, VSWR and Impedance.(Evaluate)
- 8. Design microwave links. (Create)

#### UNIT – I

**Microwave Transmission Lines:** Introduction to Microwaves, Microwave regions and bands, Applications, Rectangular Waveguides-Solution of Wave Equations in Rectangular Coordinates, TE/TM mode analysis, Expressions for Fields, Characteristics Equation and cut-off Frequencies, Dominant and Degenerate Modes, Sketches of TE and TM mode fields in the cross-section, Mode Characteristics.

#### UNIT – II

**Waveguide Components and Applications:** Coupling probes & loops, waveguide windows, Posts & Tuning Screws, Waveguide phase shifters and attenuators. Microwave Multiport Junctions – E-plane Tee, H-plane Tee and Magic Tee, Rat Race, Directional couplers, Ferrites – Composition and characteristics, Faraday rotation, Ferrite components- Gyrator, isolator, and Circulator their applications. Scattering Matrix – Significance, formulation and properties, S-matrix of waveguide Tee junctions, Directional Coupler, Circulator and Isolator.

#### $\mathbf{UNIT} - \mathbf{III}$

**Microwave Tubes:** Limitations and Losses of conventional tubes at Microwave frequencies, Microwave tubes – Classification.

**O-Type tubes:** 2 cavity Klystrons – structure, velocity modulation process and Applegate diagram, Bunching process and Small Signal Theory - Expressions for o/p Power and Efficiency. Reflex Klystrons-structure, velocity modulation and Applegate diagram, Mathematical Theory of Bunching, Power output, Efficiency, Oscillating modes and o/p characteristics, Effect of repeller voltage on Power output.

### $\mathbf{UNIT} - \mathbf{IV}$

**M-Type Tubes:** Magnetrons – Different types, cylindrical Traveling Wave Magnetron – Hull cut-off and Hartree conditions, Modes of Resonance, PI-mode and its separation, o/p characteristics.

**Microwave Solid State Devices:** Introduction, classification, Applications, TEDs-Introduction, Gunn diode-principle, RWH theory, modes of operation and characteristics, Avalanche Transit Time Devices-Introduction IMPATT diodes, TRAPATT diodes.

#### $\mathbf{UNIT} - \mathbf{V}$

**Microwave Measurements:** Description of Microwave Bench-Different blocks and their Features, Precautions; Microwave Power Measurement – Bolometer, Measurement of Attenuation, Frequency, VSWR and Impedance.

### **TEXT BOOKS:**

- 1. Samusel Y. Liao, "Microwave Devices and Circuits", PHI. ISBN-10: 0135832047
- 2. Herbert J.Reich J.G. Skolnik, P.F. Ordung and H.L. Krauss, "Microwave Principles", affiliated East West Press Pvt., Ltd., New Delhi. ISBN:81-7671-017-2

### **REFERENCE BOOKS:**

- 1. M.Kulkarni, "Microwave and Radar Engineering", *ISBN Number*: 8188114006, 9788188114009, 978-8188114009
- George Kennedy, "Electronic Communications Systems", McGraw Hill Publ. ISBN-10: 0-07-463682-0

### WEBSITES

- 1. nptel.ac.in
- 2. freevideolectures.com/Subject/Electronics.
- 3. ocw.mit.edu
- 4. <u>www.pearsoned.co.uk</u>.
- 5. <u>www.ece.uiuc.edu</u>.
- 6. www.utexas.edu
- 7. www.electron.frba.utn.edu.ar/.../Microwave\_Engineering\_David\_M\_Poz...
- 8. www.burnbits.com/.../Pozar%20-%20Microwave%20Engineering.pdf
- 9. https://ecedmans.files.wordpress.com/2014/10/microwave-devices-and-circuits-samuelliao.pdf

### **CONTENT BEYOND SYLLABUS:**

Introduction to Microwave integrated circuits.

Sl. No.	Topics in syllabus	Modules and Sub modules	Lecture No.	Suggested books with Page Nos.
UNI	Γ – I (No. of Lectures	-12)	Microw	ave Transmission Lines
1	Introduction to Microwaves	Microwave regions and bands, Applications	L1 L2	Microwave and Radar Engineering (M. Kulkarni)- (Page- 1-8)
2	Rectangular Waveguides	Solution of Wave Equations in Rectangular Coordinates	L3 L4	M. Kulkarni- 85-90 Microwave Devices and Circuits (Samual Y. Liao)-103
3	TE/TM mode analysis	Expressions for Fields, Characteristics Equation and cut-off Frequencies, Dominant and Degenerate Modes, Sketches of TE and TM mode fields in the cross- section	L5 L6 L7 L8 L9	M. Kulkarni-90- 97,105-112 Samual Y. Liao-103- 116

### **LECTURE PLAN**

ComponentsWaveguide attenuatorsInsters LifeInfer Life6Microwave Multiport JunctionsE-plane Tee, H-plane Tee and Magic Tee, Rat Race, Directional couplersL17 L18 L19M. Kulkarni-187-21 Samual Y. Liao-144 1547FerritesComposition and characteristics, Faraday rotationL20M. Kulkarni-218-214 Samual Y. Liao-144 1548Ferrite componentsGyrator, isolator, and Circulator their applicationsL21 L22M. Kulkarni-220-22 Samual Y. Liao-154 1609Scattering MatrixSignificance, propertiesformulation and propertiesL23M. Kulkarni-187-19 M. Kulkarni-187-1910Scattering MatrixSignificance, propertiesfree junctions, Directional Coupler, Circulator and Isolator.L24 L25 L26M. Kulkarni-213-21' M. Kulkarni-213-21'11Limitations classification.and Losses of requencies, Microwave tubes - Classification.M. Kulkarni-213-21' 217283-289 Samual Y. Liao-332' 336,425-42612O-Type tubes2 cavity KlystronsL29 Structure, velocity modulation process and Applegate diagram, Bunching processL31 L32 L360132 cavity KlystronsStructure, velocity modulation afficiencyL33 Samual Y. Liao-342 S6014Small Signal TheoryMathematical Theory of Bunching, Power output, Efficiency, Oscillating Power out	4			T 10		
4       Mode Characteristics       Wavelength phase velocity, group velocity,	1				M Kulkarni-90 97-	
UNIT - II (No. of Lectures - 14)Waveguide windows, Posts & Tuning Screws, Waveguide phase shifters and attenuatorsL12L13 L14 L155Waveguide componentsCoupling probes & loops, waveguide windows, Posts & Tuning Screws, Waveguide phase shifters and attenuatorsL13 L14 L15M. Kulkarni-213-21'6Microwave Multiport JunctionsE-plane Tee, H-plane Tee and Magic Tee, Rat Race, Directional couplersL17 L18 Samual Y. Liao-145 L19M. Kulkarni-218-21' Samual Y. Liao-145 L207FerritesComposition and characteristics, Faraday rotationL20M. Kulkarni-218-21' Samual Y. Liao-155 1609Scattering MatrixGyrator, isolator, and Circulator their applicationsL21 L22M. Kulkarni-218-21' Samual Y. Liao-155 1609Scattering MatrixSignificance, formulation and propertiesL23 UNIT - III (No. of Lectures -12)M. Kulkarni-213-21' Limitations and Losses of frequencies, Microwave tubes - Classification.M. Kulkarni-213-21' L17211Limitations and Classification.Limitations and Losses of frequencies, Microwave tubes - Classification.M. Kulkarni-2842 Samual Y. Liao-332' 336,425-42612O-Type tubesStructure, velocity modulation process and Applegate diagram, Bunching processL33 L360132 cavity KlystronsStructure, velocity modulation and L162L34 L36014Small Signal TheoryExpressions for o'p Power and ElficiencyL34 L3614Small Signal TheoryStructure, velocity modulation and <br< td=""><td>4</td><td>Mode Characteristics</td><td></td><td></td><td>-</td></br<>	4	Mode Characteristics			-	
5Waveguide componentsCoupling probes & loops, waveguide windows, Posts & Tuning Screws, Waveguide phase shifters and attenuatorsL13 L14 L156Microwave Multiport JunctionsE-plane Tee, H-plane Tee and Magic Tee, Rat Race, Directional couplersL17 L18 L19M. Kulkarni-187-210 Samual Y. Liao-149 1547FerritesComposition and characteristics, Faraday rotationL20M. Kulkarni-218-210 M. Kulkarni-218-2108Ferrite componentsGyrator, isolator, and Circulator their applicationsL21 L22M. Kulkarni-218-210 Samual Y. Liao-150 1609Scattering MatrixSignificance, formulation and propertiesL23M. Kulkarni-213-211 M. Kulkarni-213-211 L2210Scattering MatrixSignificance, formulation and Isolator.L24 L25M. Kulkarni-213-211 M. Kulkarni-213-21111Limitations and Classification.L24 PropertiesM. Kulkarni-213-211 Limitations and Classification.M. Kulkarni-213-211 Limitations S and Losses of Classification.M. Kulkarni-213-211 L12612O-Type tubes2 cavity Klystrons, Reflex Klystrons, Reflex KlystronsL29 Rolegate diagram, Bunching processM. Kulkarni-2842 Samual Y. Liao-343 Sa6425-426132 cavity KlystronsStructure, velocity modulation efficiencyL31 L3214Small Signal TheoryStructure, velocity modulation and Applegate diagramL34 16Small Signal TheoryMathematical Theory of Bunching, Power output, Efficiency, Oscill						
5       Waveguide Components       windows, Posts & Tuning Screws, Waveguide phase shifters and attenuators       L14 L15 L16       M. Kulkarni-213-21         6       Microwave Multiport Junctions       E-plane Tee, H-plane Tee and Magic Tee, Rat Race, Directional couplers       L17 L18 L19       M. Kulkarni-187-210 Samual Y. Liao-149 L54         7       Ferrites       Composition and characteristics, Faraday rotation       L20       M. Kulkarni-218-210 Samual Y. Liao-149 L54         8       Ferrite components       Gyrator, isolator, and Circulator their applications       L21 L22       M. Kulkarni-218-210 M. Kulkarni-218-210 Samual Y. Liao-159 L60         9       Scattering Matrix       Significance, formulation and properties       L24 L25 L26       M. Kulkarni-219-20 M. Kulkarni-219-20 Samual Y. Liao-159 L60         10       Scattering Matrix       Significance, formulation and properties, Microwave tubes, L24 L25       M. Kulkarni-213-211         11       (No. of Lectures -12)       Microwave Tube         11       Limitations and Classification.       Limitations and conventional tubes at Microwave frequencies, Microwave tubes - Classification.       L30 Samual Y. Liao-333 336,425-426         12       O-Type tubes       2 cavity Klystrons, Reflex Klystrons       L29 Structure, velocity modulation process and Applegate diagram, Bunching process       L33 L33       Samual Y. Liao-343 360         14       Small Signal Theory       Mathemati	UNI	<b>T – II</b> (No. of Lecture	s - 14) Waveg		onents and Applications	
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15       Reflex Klystrons       Applegate diagram       L35       Samual Y. Liao-373         16       Small Signal Theory       Mathematical Theory of Bunching, Power output, Efficiency, Oscillating modes and o/p characteristics, Effect of repeller voltage on Power output.       L36       382         UNIT – IV (No. of Lectures –12)			·	1.24		
16       Small Signal Theory       Mathematical Theory of Bunching, Power output, Efficiency, Oscillating modes and o/p characteristics, Effect of repeller voltage on Power output.       L36       382         UNIT – IV (No. of Lectures –12)	15	Reflex Klystrons	Applegate diagram			
16       Small Signal Theory       Mathematical Theory of Bunching, Power output, Efficiency, Oscillating modes and o/p characteristics, Effect of repeller voltage on Power output.       L36 L37 L38       382         UNIT – IV (No. of Lectures –12)				L <i></i> JJ	Samual Y. Liao-373-	
16       Small Signal Theory       Power output, Efficiency, Oscillating modes and o/p characteristics, Effect of repeller voltage on Power output.       L37         UNIT – IV (No. of Lectures –12)         M-Type Tube			•	L36		
of repeller voltage on Power output.     L38       UNIT – IV (No. of Lectures –12)     M-Type Tube	16	Small Signal Theory		L37		
UNIT – IV (No. of Lectures –12) M-Type Tube				L38		
	UNI	T – IV (No. of Lectur			M-Type Tubes	
- · · · · · · · · · · · · · · · · · · ·		, , , , , , , , , , , , , , , , , , ,	· · · · · · · · · · · · · · · · · · ·	L39		
		~			M. Kallrows: 204-224	
(vlindrice) (reveling	10	Cylindrical Traveling		L41	M. Kulkarni-324-334	
18 Wave Magnetron Modes of Resonance, PI-mode and L42 Samual Y. Liao-427 its separation, o/p characteristics. L42 441	10			L42	Samual Y. Liao-427-	
L43			no separation, o/p characteristics.	L43	<del>44</del> 1	
19 Microwave Solid Introduction, classification, L44 M.Kulkarni-	19			I 44		
<sup>19</sup> State Devices Applications 144 352,388,399	17	State Devices				
	20	TEDs	Introduction, Gunn diode-principle,		Samual Y. Liao-269-	
20 TEDs Introduction, Gunn diode-principle, L45 Samual Y. Liao-269	_0		RWH theory, modes of operation	L46	291	

		and characteristics	L47	
21	Avalanche Transit Time Devices	Introduction IMPATT diodes, TRAPATT diodes.	L48 L49 L50	M. Kulkarni-399-406
UNI	<b>Γ</b> – V (No. of Lecture	s – 10)	Mi	crowave Measurements
22	Microwave Measurements	Description of Microwave Bench- Different blocks and their Features, Precautions	L51 L52	M. Kulkarni-247
23	Microwave Power Measurement	Low, medium and high power Measurement	L53 L54	M. Kulkarni-262
24	Measurement of Attenuation	Power ratio and RF substitution method	L55	M. Kulkarni-266
25	Measurement of Frequency	Electronic method	L56	M. Kulkarni-261
26	Measurement of VSWR	Low and high VSWR Measurement	L57 L58	M. Kulkarni-270
27	Measurement of Impedance.	Using Magic T, Slotted line and reflectometer	L59 L60	M. Kulkarni-272

# **REVIEW QUESTIONS**

## **10 MARKS QUESTIONS**

## UNIT-I (Microwave Transmission Lines)

- 1. What are microwaves and Explain advantages and applications of microwaves
- 2. Derive the  $TM_{mn}$  mode field equations in a rectangular waveguide.
- 3. Formulate the expressions for cut off frequency, phase constant, group velocity, Phase velocity and wave impedance in a rectangular waveguide.
- 4. Assuming that the waves are propagating in the positive z-direction in a waveguide derive the expression for cut-off frequency of a rectangular waveguide in  $TE_{mn}$  mode.
- 5. Draw the field patterns in a rectangular waveguide.
- 6. Explain the excitations of  $TE_{10}$  and  $TM_{11}$  modes.
- 7. (a) Derive cut off frequency of a rectangular waveguide.
  - (b) A rectangular wave guide having 2 x 1 cms and operating at a frequency of 9GHz. Then calculate cut-off wave length for the dominant mode.

8. Derive expression for wave impedance in a rectangular waveguide.

- 9.(a) Derive the  $TE_{mn}$  mode field equations in a rectangular waveguide.
  - (b) A rectangular waveguide having dimensions 2.5 x 1cms and operating frequency is 8GHz. Then find number of possible modes.
- 10. Explain probe and loop coupling mechanisms with neat sketches.

## **UNIT-II (Waveguide Components)**

1. State the properties of E plane Tee and H plane Tee.

- 2. Give the properties of S –parameters and explain why S parameters used at microwave frequencies?
- 3. Show that a symmetrical magic Tee is a 3dB directional coupler.
- 4. What are microwave ferrites? Explain the working of ferrite isolator.
- 5. Derive the S-matrix of a directional coupler in standard form.
- 6. Draw magic T junction, state properties and derive its scattering matrix.
- 7. (a) Define the properties of directional coupler(b) Explain operation of two hole direction coupler
- 8. A 90 W power source is connected to the input of a directional coupler with C=25dB, D=35dB and insertion loss =0.5dB. Find the output powers at the through, coupled and isolated ports. Assume all ports to be matched.
- 9. (a) Explain the principle of ferrite phase shifter.
  - (b) Explain the principle of operation of an isolator? What is the significance of using isolator in microwave circuits?
- 10. (a) Prove that attenuation of rotary vane attenuator is  $-40 \log \cos(\theta)$
- (b) What is Faraday rotation? Construct 4-port circulator using two magic Tees and a

gyrator.

## UNIT-III (Microwave Tubes-O-Type Tubes)

- 1. What are the limitations of conventional tubes at microwave frequencies? Classify microwave tubes.
- 2. Explain the operation of two cavity klystron amplifier using applegate diagram.
- 3. Explain in detail bunching process & obtain expression for bunching parameter in a two cavity klystron amplifier.
- 4. Derive the expression for output power & Efficiency of a 2 cavity klystron.
- 5. Explain the principle of operation of a reflex Klystron oscillator and derive an expression for the bunching parameter.
- 6. Derive the relation between accelerating voltage  $V_0$ , repeller voltage  $V_R$  & repeller space L.
- 7. Show that the theoretical efficiency of reflex klystron is 27.78%.
- 8. A reflex klystron having an accelerated field of 300V oscillates at a frequency of 10GHz with a retarding field of 500V. If its cavity is returned to 9GHz. What must be the new value of retarding field for oscillations in the same mode to take place?
- 9. A reflex klystron operates at the peak mode of n = 2 with Beam voltage  $V_0 = 300V$ , Beam current  $I_0 = 20mA$ , Signal Voltage  $V_1 = 40V$ . Determine:
  - i. Input power in watts.
  - ii. Output power in watts.
  - iii. The efficiency.
- 10. A reflex klystron is under following operating conditions:  $V_0 = 600V$ , L = 1 mm,  $R_{sh}=15k\Omega$ ,  $e/m=1.759 \times 10^{11}$   $f_r = 9$ GHz. The tube is oscillating at  $f_r$  at the peak of the n = 2 mode.
  - a. Find the value of repeller voltage  $V_r$
  - b. Find the direct current necessary to give microwave voltage of 200V.

## UNIT-IV (M-Type Tubes & Solid state devices)

1. What is a Cross-field generator? Explain how  $\pi$ -mode oscillations are generated in this cross-field device.

- 2. Explain how oscillations are sustained in the Cavity Magnetron, with suitable sketches.
- 3. Derive an expression for the Hull cut off condition for cylindrical magnetron oscillator.
- 4. Derive 'Hartree' condition of a cavity type magnetron.
- 5. Explain Gunn Effect using two valley theory and explain J-E characteristics of Gunn diode.
- 6. (a)Derive the criterion for classifying the modes of operation for Gunn effect diodes.

(b)An n-type GaAs Gunn diode has following parameters Electron drift velocity:  $Vd = 2.5 \times 105m/s$ Negative Electron mobility:  $\mu n = 0.015 m^2/V s$ 

Relative dielectric constant  $\varepsilon_r = 13.1$ 

Determine the criterion for classifying the modes of operation.

- 7. Write in detail the principle mechanism of operation and the application of IMPATT diode
- 8. Describe the principle of operation of TRAPATT diode.
- 9. A Ku-band IMPATT diode has a pulse operating voltage of 100V and a pulse operating current of 0.9A. The efficiency is about 10%. Calculate
  - a. The output power
  - b. The duty cycle if the pulse width is 0.01 ns and frequency is 16 GHz.

10. Compare IMPATT and TRAPATT diodes.

#### **UNIT-V** (Microwave Measurements)

- 1. Draw a neat diagram of microwave test bench and explain about each block along with its features.
- 2. Define VSWR. Describe the methods of measuring high and low VSWRs.
- 3. Explain the measurement of unknown impedance using Smith Chart.
- 4. Explain the method of measuring impedance at microwave frequencies.
- 5. Explain the RF substitution method of measurement of attenuation.
- 6. Explain the measurement of power using bolometer method.
- 7. Explain the frequency measurement techniques.
- 8. A slotted line is used to measure the frequency and it was found that the distance between the nulls is 1.85 cm. Given the guide dimension as 3cm X 1.5 cm. Calculate the frequency.
- 9. Double minimum method is used to determine the VSWR values on a waveguide. If the separation between the two adjacent nulls is 3.5cm and that between twice minimum power point is 2.5mm. Determine the values of VSWR?
- 10. In the X-Band lab microwave test bench measurement, it is found that the distance between two successive minima is 2.5 cm. Calculate the frequency of the microwave source. Assume inside dimensions of X-Band waveguide to be 2.286 Cm x 1.016 Cm.

## **<u>2 MARKS QUESTIONS</u>**

### **UNIT-I (Microwave Transmission Lines)**

- 1. Classify the basic advantages of microwaves
- 2. How are waveguides different from normal two wire transmission lines?

- 3. List the typical applications of microwaves
- 4. Define microwaves.
- 5. Classify types of waveguides.
- 6. Draw the field pattern of  $TM_{11}$  mode of a rectangular waveguide.
- 7. Is the waveguide a High pass filter? If yes, Justify.
- 8. If a metallic cylindrical post is introduced into the broader side wall of a wave guide

and the post extends only a short distance  $<\frac{\lambda_g}{4}, =\frac{\lambda_g}{4}, >\frac{\lambda_g}{4}$  respectively .Draw the

electrical equivalent circuits of all the cases.

- 9. Define guide wavelength in a rectangular waveguide.
- 10. Define wave impedance in a rectangular waveguide.
- 11. Define phase velocity and group velocity.
- 12. List out microwave sub bands.
- 13. Define dominant mode.
- 14. Define degenerate modes
- 15. Define cut-frequency of a rectangular waveguide.

## **UNIT-II (Waveguide Components)**

- 1. Define a microwave junction.
- 2. Define S-matrix or scattering matrix.
- 3. Why the s-parameters are used in microwaves?
- 4. What is Tee junction? Give two examples
- 5. What is H-Plane Tee?
- 6. What is E- plane Tee?
- 7. Give a note on directional coupler.
- 8. What are the Properties of s-matrix?
- 9. What are the properties of scattering matrix for a lossless junction?
- 10. Give the applications of directional coupler
- 11. What are junctions? Give some examples
- 12. What is hybrid ring?
- 13. What are the different types of Directional couplers?
- 14. What are the three properties of an ideal directional coupler?
- 15. What is the role of "magic T" in measuring the impedance?
- 16. State the 'Phase shifting' property of S- parameters.
- 17. Write principle of operation of a circulator.
- 18. Calculate the attenuation of a rotary vane attenuator if the angle of rotation is 30

degrees.

19. What is the function of isolator in microwave bench setup?

## UNIT-III (Microwave Tubes-O-Type Tubes)

- 1. What are the high frequency effects in conventional tubes?
- 2. Give the drawbacks of klystron amplifiers.
- 3. What is the effect of transit time?
- 4. What are the applications of reflex klystron?
- 5. How the klystron amplifier can act as klystron oscillator? What are the applications of klystron amplifier?
- 6. Define phase focusing effect.
- 7. What do you mean by O-type tubes? Name some O-type tubes.

- 8. Define Transit time in Reflex klystron.
- 9. Give the performance Specification of Reflex klystron?
- 10. State the characteristics of 2-cavity klystron amplifier.
- 11. What do you meant klystrons?
- 12. Define velocity modulation?
- 13. Mention the applications of two cavity klystron.
- 14. What is drift space?
- 15. Define bunching.
- 16. What are the differences between klystron amplifier and Reflex klystron?
- 17. For a two-cavity klystron, the spacing between the centers of cavities is 4cm and the beam voltage is 900V.Find the velocity and DC transit time of electron.
- 18. Draw the electronic admittance spiral of Reflex klystron.

### UNIT-IV (M-Type Tubes & Solid state devices)

- 1. State the characteristics of magnetron.
- 2. State the applications of magnetrons. Why magnetron is called as cross filed device?
- 3. What is frequency pulling and frequency pushing in magnetrons?
- 4. What is strapping. Why it is required in a Magnetron? What are the disadvantages of strapping?
- 5. What are the Key phenomenon taking places in TRAPATT diode?
- 6. What is the operating frequency of TRAPATT devices?
- 7. What are the applications of TRAPATT devices?
- 8. What are the elements that exhibit Gunn Effect?
- 9. What are the applications of Gunn Diode?
- 10. What is negative resistance?
- 11. What is the main advantage of TRAPATT over IMPATT?
- 12. Define GUNN EFFECT
- 13. Explain stable amplification mode.
- 14. Explain plasma formation in TRAPATT diode.
- 15. What is negative resistance in Gunn diode?
- 16. What are the applications of TRAPATT?
- 17. What is Transferred electron effect?
- 18. What are the various modes of transferred electron oscillators?
- 19. Differentiate baretter and thermistor?
- 20. What are the applications of IMPATT diode?
- 21. Define negative resistance related to microwave sources.

### **UNIT-V (Microwave Measurements)**

- 1. What are tunable detectors?
- 2. What is slotted section with line carriage?
- 3. What is the main purpose of slotted section with line carriage?
- 4. What is a VSWR meter?
- 5. What is Bolometer?
- 6. What is calorimeter?
- 7. How will you determine the VSWR and return loss in Reflecto meter method?
- 8. List the different types of Impedance measurement methods?
- 9. How do you measure microwave frequency?
- 10. What is a wave meter?
- 11. Distinguish between low frequency measurements and microwave measurements.
- 12. Explain the attenuation measurements?

- 13. Why bolometer method is not suitable for the measurement powers greater than 10mW.
- 14. Why slot is located at the center of the slotted section?
- 15. What are low VSWR and high VSWR and name the method followed to measure high VSWR?

### (13EC428) VLSI DESIGN

### **Course Description:**

VLSI design is to study the process of implementing a digital system as a CMOS integrated circuit. The course will begin with a review of the basics of CMOS transistor operation and the manufacturing process for CMOS VLSI chips. Next detail the problem of implementing logic gates in CMOS. Specifically, cover layout, design rules, and circuit families. Afterwards, examine techniques for timing and power analysis and clocking. Also examine ways to optimize timing and power. This will be followed by an overview of data path design, specifically adders and multipliers and study memory arrays, including SRAM and DRAM cell and clock design. The course will conclude with CMOS testing need for testing, test principles, design strategies for test, design for test and system-level test techniques layout design for improved testability.

### **Prerequisites**

Pre-requisite: Digital Electronics .

### **Course Objectives**

- 1. Comprehends the basic IC technologies viz. PMOS, NMOS, CMOS and BiCMOS.
- 2. Interprets MOS device concepts and draw stick diagrams and layouts using design rules.
- 3. Impart design skills of various logic styles and evaluation of delays etc.
- 4. Interprets subsystems design concepts and semi-custom IC design options.
- 5. Explains the various CAD tools and testing of VLSI circuits.

### **COURSE OUTCOMES:**

The students will be able to

- 1. Describes fabrication steps of IC
- 2. Explains Ids vs Vds relation for a MOS Transistor
- 3. Distinguishes NMOS Inverter And CMOS Inverter
- 4. Comprehends MOS device concepts , draw stick diagrams and layouts using design rules
- 5. Comprehends gate level design
- 6. Design digital systems and components
- 7. Describes semiconductor integrated circuits design
- 8. Explains test Principles and different testing methods

## **SYLLABUS**

## UNIT – I

**Introduction:** Introduction to IC Technology – MOS, PMOS, NMOS, CMOS, BiCMOS & GaAs.

**Basic Electrical properties**:  $I_{ds} - V_{ds}$  relationship,  $V_t$ ,  $g_m$ ,  $g_{ds}$ ,  $\omega_0$  (figure of merit) pass transistor, NMOS inverter, various pull ups, CMOS inverter analysis and design, Bi- CMOS Inverters.

### UNIT – II

**MOS and BICMOS Circuit Design Process:** MOS layers, stick diagrams, design rules and layout, 2 µ meter CMOS design rules, layout diagrams, VLSI Design Flow.

**Basic circuit concepts:** sheet resistance, Area capacitance of layers, delay unit, wiring capacitance, choice of layers.

Scaling of MOS circuits: Scaling models, scaling function for device parameters, limitations of scaling.

### UNIT – III

**Gate Level Design:** Logic gates & other complex gates, switch logic, alternate gate circuits, fan in-fan out.

Semi conductor IC design: PLA, PAL, FPGAs, CPLDs, Standard Cells, Low Power Design.

### $\mathbf{UNIT} - \mathbf{IV}$

**Data Path Subsystems:** Subsystem Design, shifters, adders, ALUs, multipliers, parity generators, comparators, zero/one detectors, counters.

Array subsystems: SRAM, DRAM, ROM, Serial Access Memories, content addressable memory.

## UNIT – V

**CMOS Testing:** CMOS testing need for testing, test principles, design strategies for test, chip level test techniques, system-level test techniques layout design for improved testability.

### **TEXT BOOKS:**

- 1. K.Eshraghian, Eshraghian Dougles and A. Pucknell, "Essentials of VLSI circuits and systems", PHI 2005 Edition. ISBN: 978-81-203-2772-6
- 2. Neil H.E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design A circuits and systems perspective", Pearson, 2009. ISBN 13: 978-0-321-54774-3
- 3. Neil H.E. Weste, K.Eshraghian, "Principles of CMOS VLSI Design ", Pearson, 2009. ISBN 13: 978-0-321-54774-3

## **REFERENCE BOOKS:**

- 1. Wayne Wolf, "Modern VLSI Design", Pearson education, 3<sup>rd</sup> edition. 1997. ISBN-10: 0137145004 | ISBN-13: 978-0137145003
- 2. Mead, C.A and Convey,L.A, "Introduction to VLSI systems", Wesley-Wesley. ISBN-10: 0201043580 | ISBN-13: 978-0201043587
- 3. Charles H.Roth, Jr, Lizy Kurian John "Digital systems design"2<sup>nd</sup> Edition Cengage Learning.
- 4. John M. Rabaey,"Digital Integrated Circuits" PHI, IEEE, 1997.
- 5. John .P. Uyemura "Introduction to VLSI Circuits and Systems ", JohnWiley, 2003.

## WEBSITES

- 1. www.csee.umbc.edu/~cpatel2/links/315/lectures/chap1\_lect00\_intro.pdf
- 2. www.hindawi.com/journals/vlsi/guidelines/
- 3. www.cin.ufpe.br/~mel/pub/prototipacão/referencias/...design/CMOS-VLSIdesign.pdf
- 4. web.ewu.edu/groups/technology/Claudio/ee430/Lectures/L1-print.pdf
- 5. <u>www.tutorialspoint.com/vlsi\_design/vlsi\_design\_tutorial.pdf</u>
- 6. www.facweb.iitkgp.ernet.in/~isg/CAD/SLIDES/06-VLSI-design-styles.pdf

## **CONTENT BEYOND SYLLABUS:**

Need for Low Power Circuit Design, Sources of Power Dissipation

## LECTURE PLAN

Sl. No.	Topics in syllabus	Modules and Sub modules	Lecture No.	Suggested books with Page Nos.
UNIT	<b>I – I: (No. of Lecture</b>	s – 15)		
1	Introduction to IC Technology – MOS	Introduction to IC , IC era, MOS related VLSI technology	L1	T1-2 T1-4 T1-6
2	NMOS	Basic MOS transistors Enhancement mode, Depletion mode ,	L2 L3	T1-6 T1-9 T1-10
3	PMOS	Enhancement mode, Depletion mode	L4	T1-8 T1-10
4	NMOS Fabrication steps	NMOS Fabrication steps	L5	T1-10
5	CMOS Fabrication steps	CMOS Fabrication steps	L6	T1-15
6	BiCMOS Fabrication steps and GaAs.	BiCMOS Fabrication steps and GaAs.	L7	T1-24
Basi	c Electrical properties	S		
7	$I_{ds}$ – $V_{ds}$ relationship,	Ids versus Vds relationships	L8	T1-29
8	$V_t, g_m, g_{ds}$	MOS transistor threshold Voltage Vt, Transconductance gm and gds	L9	T1-34 T1-35
	NMOS inverter	NMOS inverter and transfer characteristics	L10	T1-38
9		Determination of Zp.u/Zp.d for an NMOS inverter driven by another Nmos transistor ZP.u/Zp.d for an NMOS inverter	L11	T1-40
		driven through one or more transistors Alternative forms of pull-up	L12	T1-42
			L 10	T1-45
10	CMOS inverter analysis and design	CMOS inverter analysis and design.	L13	T1-47
11	Bi- CMOS Inverters.	Bi- CMOS Inverters	L14	T1-54
		Latch-up in CMOS circuits	L15	T1-57
UNIT	□ –II :MOS and BICN	AOS Circuit Design Process (No. o	of Lectures	- 11)

12	VLSI Design Flow.	VLSI Design Flow.	L16	T2-430
13	MOS layers, stick diagrams	MOS Layers, nMOS, CMOS design styles	L17 L18	T1-62 T1-62
14	Design rules	Lambda based Design rules Contact cuts CMOS Lambda based Design rules	L19 L20	T1-72 T1-75 T1-78
		Transistors layout diagrams for NMOS inverter and gates	L21	T1-84
15	Layouts	layout diagrams for CMOS inverter	L22	T1-COLOR plates
		NAND,NOR and other gates	L23	T1-COLOR plates
16	Basiccircuitconcepts:sheetresistance,Areacapacitanceoflayers,	sheet resistance, Area capacitance of layers,	L24	T1-95 T1-99
17	Delay unit, wiring capacitance, choice of layers.	Delay unit, wiring capacitance, choice of layers.	L25	T1-102 T1-118
18	Scaling of MOS circuits: Scaling models, scaling function for device parameters, limitations of scaling.	Scaling models, scaling function for device parameters Limitations of scaling.	L26	T1-124 T1-129
UNIT	r – III : Gate Level Do	esign (No. of Lectures – 06)		
19	Logic gates & other complex gates	Logic Gates and Other complex gates	L27	T1-149
20	switchlogic,alternategatecircuits,fan in, fan out	Switch logic with pass transistors and Transmission gate	L28	T1-148
21	Semi conductor IC design: PLA, PAL	PLA,	L29	R3-146
22	FPGAs, CPLDs	PAL FPGAs, CPLDs	L30 L31	R3-151 R3-156 R3-160
23	Standard Cells, Low Power Design.	Standard Cells, Low Power Design.	L32	T2- 303
UNIT	<b>[] –IV: Data Path Sub</b>	systems (No. of Lectures - 11)		
24	Adders	Adders		T2-303

			L33			
25	Shifters	Shifters	L34	T2-343		
26	ALUs, multipliers	ALUs, multipliers	L35 L36	T2-345		
27	parity generators, comparators, zero/one detectors, counters	parity generators, comparators, zero/one detectors, counters	L37 L38	T2-340 T2-331 T2-330 T2-332		
28	Array subsystems: SRAM	SRAM	L39	T2-369		
29	DRAM	DRAM	L40	T2-385		
30	ROM, Serial Access Memories,	ROM, Serial Access Memories,	L41	T2-389 T2-393		
	content addressable memory.	Content addressable memory.	L42	T2-395		
UNI	UNIT – V: CMOS Testing((No. of Lectures – 11)					
31	Need for testing	Introduction Need for testing	L43	T3-465 T3-465		
			L44			
32	test principles, design strategies for	Test Principles, Design Strategies for test	L45 L46	T3-471 T3-485		
	test					
		chip level test techniques	L47	T3-498		
33	chip level test techniques	chip level test techniques chip level test techniques	L48	T3-498		
			L49	T3-498		
	system-level test	System-level Test Techniques	L50	T3-500		
34	techniques	System-level Test Techniques	L51	T3-500		
35	layout design for improved testability.	layout design for improved testability.	L52 L53	T3-508 T3-508		

## Note

T1. TEXT BOOK 1 T2. TEXT BOOK 2 T3. TEXT BOOK 3 **R3. REFERENCE TEXT B00K 3** 

## <u>Assignment –I</u>

- Explain NMOS working with neat diagrams.
   Explain CMOS Fabrication steps.
   Explain working of CMOS inverter with transfer characteristics.

- 4. Draw stick diagrams and layout diagrams for(a) CMOS inverter, (b)NAND,(c) NOR.
- 5. Explain Switch logic with pass transistors and Transmission gate.

## <u>Assignment –II</u>

- 1. Draw architecture and explain about FPGA
- 2. Write differences between SRAM and DRAM
- 3. Draw full adder circuit with all CMOS logics
- 4. Explain driving large capacitive loads
- 5. Write about design strategies for test of VLSI circuits.

### **Review Questions**

## UNIT-I

- 1. What is the other name for MOSFET? Why is it called so?
- 2. What are the two substructures of MOSFET?
- 3. Draw the symbols for P-channel and N-channel DE-MOSFET and E-only MOSFET.
- 4. List the factors on which threshold voltage depends?
- 5. What are the different regions of operation for MOS transistors and the conditions for each?
- 6. What are the main CMOS fabrication technologies available?
- 7. What is a thinox?
- 8. What are the four basic layers on which MOS circuits are formed?
- 9. Compare CMOS and Bipolar technologies?
- 10. Compare Enhancement mode and Depletion mode MOSFET.
- 11. What factors cause punch through condition in MOS transistors?
- 12. Draw the structure of NMOS transistor.
- 13. List out the advantages of BiCMOS technology.
- 14. Compare NMOS and CMOS Technologies.
- 15. Distinguish NMOS and PMOS device characteristics?
- 16. Why NMOS technology is preferred more than PMOS technology?
- 17. What is the special feature of Twin-Tub process?
- 18. Give the basic process for IC fabrication.
- 19. What are the different operating regions of MOS transistor?
- 20. List the factors which affect the threshold voltage of a MOS transistor
- 21. Draw the model transfer characteristics for DE-MOS and E-only MOSFET
- 22. What are the main CMOS fabrication technologies available
- 23. What are the advantages of CMOS process?
- 24. Explain the following terms related to the fabrication of IC
  - a. Diffusion
  - b. Oxidation
  - c. Lithography
  - d. Metallization.
- 25. Briefly discuss the steps involved in the manufacturing process of an IC.
- 26. Give the CMOS inverter DC transfer characteristics and operating regions ?
- 27. Draw the circuit of a NMOS, CMOS inverter?
- 28. Write the equation for threshold voltage and the significance of MOS transistor transconductance?
- 29. Discuss different parameters on which threshold voltage depends?
- 30. Discuss the CMOS invertors transfer characteristics.
- 31. How latch up problems can be rectified in BICMOS fabrication process?

- 32. Give the expression for power dissipation in CMOC inverter.
- 33. Implement NAND gate using CMOS.
- 34. Define gain factor of MOS transistor.
- 35. What are the four possible arrangements of pull-up?
- 36. What is the condition for pull up to pull down ratio of an inverter? (a) directly from the output of another inverter (b) through one or more pass transistors.
- 37. Mention with necessary conditions why NMOS is used as pull down device and PMOS is used as pull up device.
- 38. Define body effect?
- 39. Sketch the Ids versus Vds graph for enhancement mode device.
- 40. What is channel length modulation of a MOSFET.
- 41. Explain figure of merit of MOS transistor.
- 42. Derive the NMOS inverter transfer characteristics.
- 43. Explain the possibility of using a CMOS inverter as an amplifier
- 44. Is the transmission of logic 1 degraded as it passes through a nMOS pass transistor? Why?
- 45. What are the advantages and disadvantages of CMOS pass transistor?
- 46. The W/L ratio of pull up of an inverter is ½ and that of the pull down is ¼. Determine the pull up to pull down ratio for this inverter.

### ESSAY QUESTIONS

- 1. With neat diagram explain MOS Transistor theory and its processing technology.
- 2. Explain the operation of nMOS Enhancement and Depletion mode transistor.
- 3. Draw the structure of pMOS and nMOS transistor and explain its working.
- 4. With a neat diagram explain the fabrication of nMOS transistor.
- 5. Explain the fabrication of pMOS transistor and its substrate fabrication process.
- 6. Explain P-well and N-well fabrication process of CMOS inverter.
- 7. Explain Twin Tub process of CMOS fabrication in detail.
- 8. Describe the important processing steps and masks for BiCMOS fabrication technology
- 9. Derive the Threshold voltage for nMOS Enhancement transistor.
- 10. Explain NMOS working with neat diagrams.
- 11. Explain CMOS Fabrication steps.
- 12. Derive an expression for nMOS transistor current equation.
- 13. Explain about the body effect of MOS transistors.
- 14. Compare CMOS and Bipolar technology.
- 15. Explain substrate bias effect.
- 16. Explain working of CMOS inverter with transfer characteristics.
- 17. Draw and discuss the MOS transistor Model.
- 18. Derive the Ids versus Vds relation for enhancement mode device.
- The W/L ratio of pull up of an inverter is <sup>1</sup>/<sub>2</sub> and that of the pull down is <sup>1</sup>/<sub>4</sub>.
   Determine the pull up to pull down ratio for this inverter.
- 20. Explain MOS transistor transconductance  $g_m$  and output conductance  $g_{ds.}$
- 21. Derive an expression for pull up to pull down ratio of an NMOS inverter driven by another NMOS inverter
- 22. Derive an expression for pull up to pull down ratio of an NMOS inverter driven by one

or more pass transistors.

- 23. Explain CMOS Inverter with neat diagram.
- 24. Explain alternative forms of pull-ups?
- 25. Explain BICMOS Inverter with neat diagram.
- 26. Explain Latchup ? and BICMOS Latch up susceptibility?

### UNIT-II

- 1. What is a stick diagram and Draw the stick diagram for NMOS inverter
- 2. What is Lambda (O) based design rules, State the significance of lambda based rule.
- 3. Design a stick diagram for two input n-MOS NAND and NOR gates.
- 4. What is a stick diagram and explain about different symbols used for components in stick diagram.
- 5. . Draw the stick diagram and layout for (a) NMOS inverter. (b) P-Well CMOS inverter.
- 6. Draw the following transistors using lambda based design rules
- i. NMOS enhancement
- ii. NMOS depletion
- iii. PMOS enhancement.
- 7. Discuss the design rules for wires (both NMOS and CMOS) using lambda based design rules.
- 8. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.
- 9. What is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
- 10. (a) What are the effects of scaling on Vt? (b) What are design rules? Why is metalmetal spacing larger than poly -poly spacing.
- 11. (a) Discuss the rule for n well and VDD and Vss contacts (2µm CMOS)

## ESSAY QUESTIONS

- 1. Draw and explain the NMOS and CMOS lambda based design rules for transistors and wires.
- 2. Draw the stick diagram for (i) 3-input NOR gate (ii) CMOS inverter.
- 3. Draw stick diagrams and layout diagrams for(a) CMOS inverter, (b)NAND,(c) NOR.
- 4. Explain the operation of inverting and non -inverting type NMOS super buffer
- 5. Draw and implement NAND and NOR logic using BiCMOS transistor.
- 6. With neat schematic explain pass transistor driving capacitive load and Inverter.
- 7. Explain the VLSI design flow with a neat diagram
- 8. Derive the scaling factor for the following
  - i. Gate area,
  - ii. Gate capacitance,
  - iii. Carrier density in channel,
  - iv. parasitic capacitance,
  - v. channel resistance,
  - vi. gate delay,
  - vii. maximum operating frequency,
  - viii. saturation current,
  - ix. current density,
  - x. switching energy per gate,
  - xi. power dissipation per gate,
  - xii. Power speed product.

- 8. Briefly explain the limitations of scaling?
- 9. Explain various circuit concepts
  - i. sheet resistance,
  - ii. Area capacitance of layers,
  - iii. delay unit,
  - iv. wiring capacitance,
  - v. Choice of layers.

### UNIT-III

- 1. What is a PLA?
- 2. What is an FPGA?
- 3. Distinguish between PLA and PAL.
- 4. List out the advantages of FPGA.
- 5. Give the difference between FPGA and CPLD.
- 6. Compare FPGA and PLA.
- 7. List the methods of programming PAL.
- 8. Why PLA's are not used in CMOS logic circuits?
- 9. Define CLB.
- 10. What is meant by an NMOS PLA?
- 11. Differentiate between PAL & PLA?
- 12. What is a LUT?
- 13. Give the difference between CPLD & FPGA?
- 14. Explain the methods of programming of PAL CMOS device.
- 15. Draw and explain the architecture of an FPGA
- 16. What are different classes of Programmable CMOS devices? Explain them briefly.
- 17. What is the basis for standard-cell? What are basic classes of circuits for Library cells? What are the advantages and disadvantages of the reconfiguration.
- 18. Mention different advantages of Anti fuse Technology.
- 19. What are different typically available SSI Standard-cell types and compare them.
- 20. Draw the diagram of programmed I/O pad and explain how the antifuses are used in this.
- 21. Draw and explain the AND/OR representation of PLA.
- 22. Sketch a 3-input, 2- output PLA implementing this logic.
- 23. Sketch a diagram for two input XOR using PLA and explain its operation with the help of truth table.
- 24. Draw various alternative gate circuits?
- 25. What are Programmable Interconnects?
- 26. What are macros?
- 27. What are the different levels of design abstraction at physical design?
- 28. Give the steps in ASIC design flow.
- 29. Describe precharge and evaluation operations associated with dynamic CMOS logic with neat diagrams.

## ESSAY QUESTIONS

- 1. Explain the general architecture of FPGA and clearly bring out the different Programmable blocks used.
- 2. Write the significance of PLA in VLSI design with neat diagram
- 3. With neat sketch explain the CLB, IOB and programmable interconnects of an FPGA

- 4. Draw and explain the general architecture of PAL device.
- 5. With neat sketch explain the CPLD?
- 6. Draw the architecture and explain about FPGA
- 7. Write the significance of Low Power Design?

## **Unit-IV**

- 1. What are data path circuits?
- 2. What is anti-fuse technique? Mention its significances.
- 3. Draw SRAM and differentiate SRAM and DRAM
- 4. What is 4\*4 carry save multiplier?
- 5. Draw content addressable memory and specify the blocks in it?
- 6. Where is Serial Access Memories applicable?
- 7. Explain the following circuits.1.Data path circuits 2.Any one adder circuit.
- 8. Draw the schematic of Pseudo-nMOS comparator.

## ESSAY QUESTIONS

- 1. Show the basic RAM architecture and explain its operation.
- 2. Design a comparator using XNOR and AND gate and draw its schematic.
- 3. Design a zero/one detector and draw its schematic and also calculate its delay.
- 4. Design a magnitude comparator based on the data path operators.
- 5. Draw the Schematic and mask layout of array adder used in Booth Multiplier and explain the principle of multiplication in Booth Multiplier.
- 6. Explain how the transistor might be sized to optimize the delay through the carry stage in parallel adder.
- 7. Design a two input XOR using a ROM.
- 8. What are the different types of Memory elements? Compare them with respect to CMOS
- 9. Explain in brief about subsystem shifters.
- 10. Explain how the partial products are independently computed in parallel multiplier.
- 11. Draw the circuit and layout for ROM and explain how the dynamic power dissipation is minimized.
- 12. Design a 4 bit barrel shifter using multiplexer.
- 13. Explain the design of a bit serial adder.
- 14. Design a 3 bit barrel shifter.
- 15. Explain the structure of a booth multiplier and list its advantages.
- 16. Give the general arrangement of a 4-bit arithmetic processor and design a 4-bit adder unit for ALU sub system.
- 17. Design a 4 bit barrel shifter.
- 18. What is 4\*4 carry save multiplier .Calculate the critical path delay.
- 19. Explain the following circuits.1.Data path circuits 2.Any one adder circuit.

## Unit-V

- 1. What are the different types of CMOS testing?
- 2. What is the need for testing?
- 3. List the system-level test techniques?
- 4. Write the chip-level test techniques?
- 5. What type of defects are tested in manufacturing testing methods?
- 6. What type of faults can be reduced by improving layout design?
- 7. Write the examples of functionality test of a chip?

8. What are the categories of Design for testability?

## ESSAY QUESTIONS

- 1. Explain how function of system can be tested.
- 2. Explain any one of the method of testing bridge faults.
- 3. What type of faults can be reduced by improving layout design?
- 4. Why the chip testing is needed? At what levels testing a chip can occur?
- 5. Explain the gate level and function level of testing.
- 6. Explain the following with respect to CMOS testing:
  - (a) ATPG
  - (b) Fault simulation
  - (c) Statistical Fault Analysis
  - (d) Fault Sampling.
- 7. What type of defects is tested in manufacturing testing methods?
- 8. Explain the manufacturing test of a chip with suitable examples.
- 9. Explain how an Ad-hoc test technique used to test long counters.
- 10. Explain the gate level and function level of testing.
- 11. Why stuck-at faults occur in CMOS circuits? Explain with suitable logical diagram and layout.
- 12. Explain how function of system can be tested.
- 13. Explain any one of the method of testing bridge faults.
- 14. Write about design strategies for test of VLSI circuits.
- 15. Explain the functionality test of a chip with suitable examples.
- 16. What are the categories of Design for testability? Explain them briefly.